# Micromachined Components for RF Systems

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# MICROMACHINED COMPONENTS FOR RF SYSTEMS

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*In the memory of*
*my late father,*

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# SUMMARY

Several fabrication techniques for surface micromachined 3-D structures have been developed for RF components. The fabrication techniques all have in common the use of epoxy patterning and subsequent metallization. Techniques and structures such as embedded conductors, epoxy-core conductors, a reverse-side exposure technique, a multi-exposure scheme, and inclined patterning are presented. The epoxy-core conductor technique makes it easy to fabricate high-aspect-ratio (10-20:1), tall (~1mm) RF subelements as well as potentially very complex structures by taking advantage of advanced epoxy processes. To demonstrate feasibility and usefulness of the developed fabrication techniques for RF applications, two test vehicles are employed. One is a solenoid type RF inductor, and the other is a millimeter wave radiating structure such as a W-band quarter-wavelength monopole antenna. The embedded inductor approach provides mechanical robustness and package compatibility as well as good electrical performance. An inductor with a peak Q-factor of 21 and an inductance of 2.6nH at 4.5GHz has been fabricated on a silicon substrate. In addition, successful integration with a CMOS power amplifier has been demonstrated. A high-aspect-ratio inductor fabricated using epoxy–core conductors shows a maximum Q-factor of 84 and an inductance of 1.17nH at 2.6GHz on a glass substrate with a height of 900 μm and a single turn. Successful W-band monopole antenna fabrication is demonstrated. A monopole with a height of 800 μm shows its radiating resonance at 85 GHz with a return loss of 16 dB.

In addition to the epoxy-based devices, an advanced tunable ferroelectric device architecture is introduced. This architecture enables a low-loss conductor device; a reduced intermodulation distortion (IMD) device; and a compact tunable LC module. A single-finger capacitor having a low-loss conductor with an electrode gap of 1.2μm and an electrode thickness of 2.2μm (1.8:1 gap aspect ratio) has been fabricated using a reverse-side exposure technique, showing a tunability ($T=100\times(C_0-C_{bias})/C_0$) of 33% at 10V. It shows an improved Q-factor of 21.5 compared with that of a 0.2μm thick capacitor, which shows a Q-factor of 9.3. Reduced IMD capacitors consist of wide RF gaps and narrowly spaced high resistivity electrodes with a gap of 2μm and a width of 2μm within the wide gap. A 14 μm gap and a 20 μm gap capacitor show improved IMD performance compared to a 4 μm gap capacitor by 6 dB and 15 dB, respectively, while the tunability is approximately 21 % at 30 V for all three devices due to the narrowly spaced multi-pair high resistivity DC electrodes within the gap. Finally, a compact tunable LC module is implemented by forming the narrow gap capacitor in an inductor shape. The resonance frequency of this device is variable as a function of DC bias and a frequency tunability of 1.1 %/V is achieved. The RF components developed in this thesis illustrate the usefulness of the application of micromachining technology to this application area, especially as frequencies of operation of RF systems continue to increase (and therefore wavelengths continue to shrink).

# CHAPTER I

# INTRODUCTION

During the past decade, the wireless communication world has increasingly exploited integration technologies. Advanced integration technologies for radio frequency (RF) systems make wireless products more compact, lighter, smaller, and more cost-effective, while their performance remains the same or is even better.

One approach to RF system integration is to build all the RF systems on a single chip; this is called system-on-a-chip (SOC). While the starting point of SOC technology is based on advances in integrated circuit (IC) fabrication, its full realization requires in-depth expertise across a variety of disciplines as well as the knowledge to successfully integrate these disciplines, including an optimization in architecture, design, and fabrication.

From the fabrication point of view, the integration of active components in RF systems has paralleled the rapid progress of IC technology, resulting in the fact that the active components of RF systems currently occupy only a small fraction of board real estate. However, passive components have not advanced in a similar manner, in part because of geometrical scaling limitations governed by operating frequency; and in part

by the lack of mature fabrication technologies for high quality factor (Q-factor) passive integration. Currently, the integration of passive components has become a bottleneck for further miniaturization and performance improvements in RF systems.

An approach to provide feasible integrated passive components is to adopt an advanced 3-D microelectromechanical systems (MEMS) fabrication technology to build RF components, by which we can expect to have RF devices with superior performance to that of conventional counterparts, while simultaneously reducing the total area required for the system. In addition, application of the 3-D MEMS technologies is not limited to RF passive components, but can be extended to the fabrication of integrable radiating structures such as millimeter wave antennas, in which the required structure dimension is in the size range of the structures achievable using 3-D MEMS technologies.

In this thesis, advanced micromachined 3-D fabrication technologies and architectures for RF components are introduced and their applications to both fixed and tunable passive components, as well as radiating structures, are demonstrated.

## 1.1. Passive Components for RF Communication Systems

In order to more clearly illustrate the type, number, and location of passive components in typical RF systems, a system-level schematic of a generic wireless RF communication system (a typical superheterodyne transceiver) is shown in Figure 1.1 [1]. While several constituent components such as low noise amplifiers, power amplifiers, mixers, and modulators are integrated using an integrated circuit transistor technology such as silicon bipolar, CMOS, GaAs, or SiGe technology, most of passive components

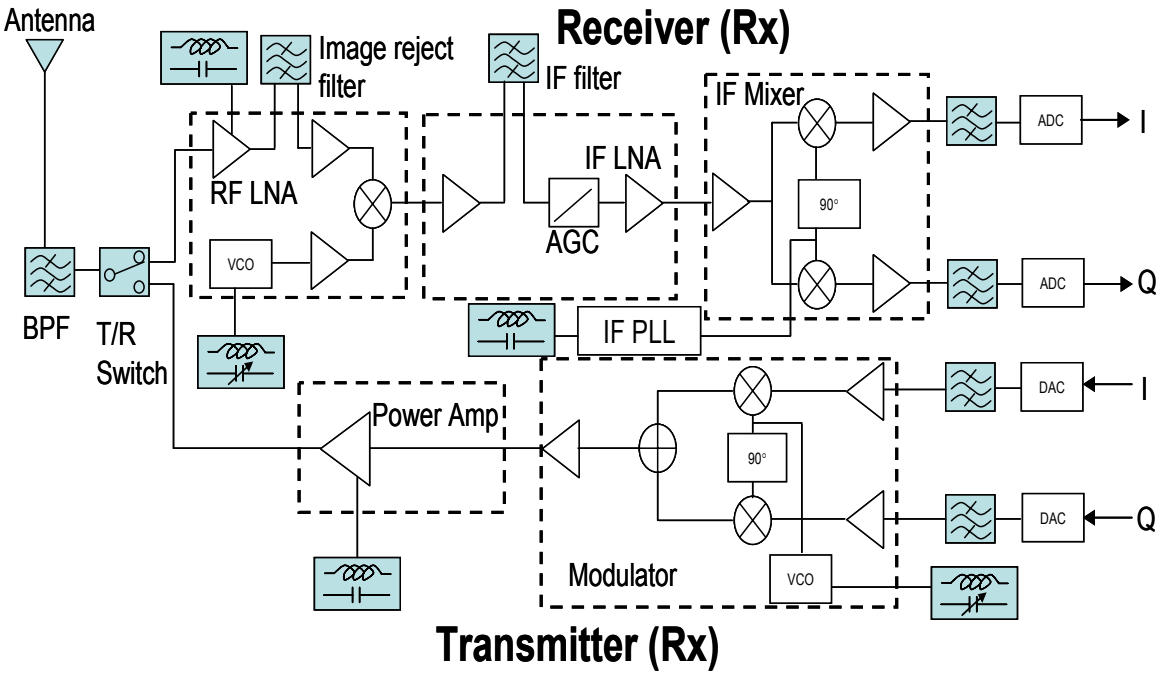


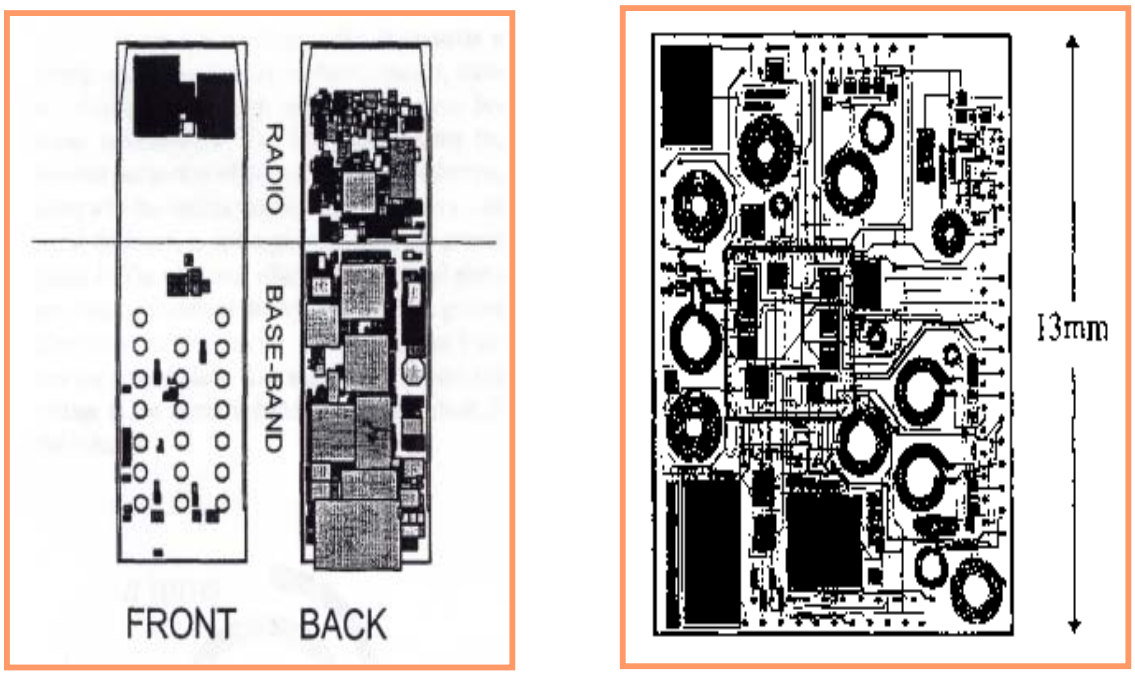

***Figure 1.1.*** *System-level schematic of a typical superheterodyne wireless transceiver [1].*

in the shaded areas of Figure 1.1 are in general excluded from the integration. Passives such as inductors, capacitors, or variable inductors used for various filters, frequency controlling devices, matching circuits, or loads are usually connected to the board as off-chip devices using flip-chip bonding or wirebonding techniques, taking a large portion of available real-estate and producing large parasitics.

Figure 1.2a shows a circuit board design example of a cellular phone handset, where only 10 % of the components are active out of a total of 375 components [2]. The remaining components consist mainly of mostly discrete inductors, capacitors, and resistors. The board is divided into two parts: a baseband section and a radio section. In the radio section, 93 % of the board space is occupied by passive components in Figure

1.2b. Clearly, it is necessary to develop integration techniques for passive components to achieve ultracompact, cost effective RF wireless systems.

Several technology development guidelines for integrated passive components are available from the literature. Figure 1.3 shows a portion of potential solutions applicable to integrated passive devices, as provided by the International Technology Roadmap for Semiconductors (ITRS) 2001 and 2003 [3]. Copper is considered as a good conductor material due to its low electrical resistivity and low material cost. While silicon dioxide ($SiO_2$) and silicon nitride ($Si_3N_4$) are currently used as standard dielectric layers for integrated capacitors, tantalum oxide ($Ta_2O_3$), barium strontium titanate (BST: $Ba_{1-x}Sr_xTiO_3$), and piezoelectric materials are being developed as potential solutions because of their high dielectric constant and low dielectric loss. For the integrated inductor, spiral,




(a) (b)

***Figure 1.2.*** *Example design of a cellular telephone: (a) Print wiring board (PWB) of inside cellular phone; (b) Multi-chip-module (MCM) layout of the radio part [2].*

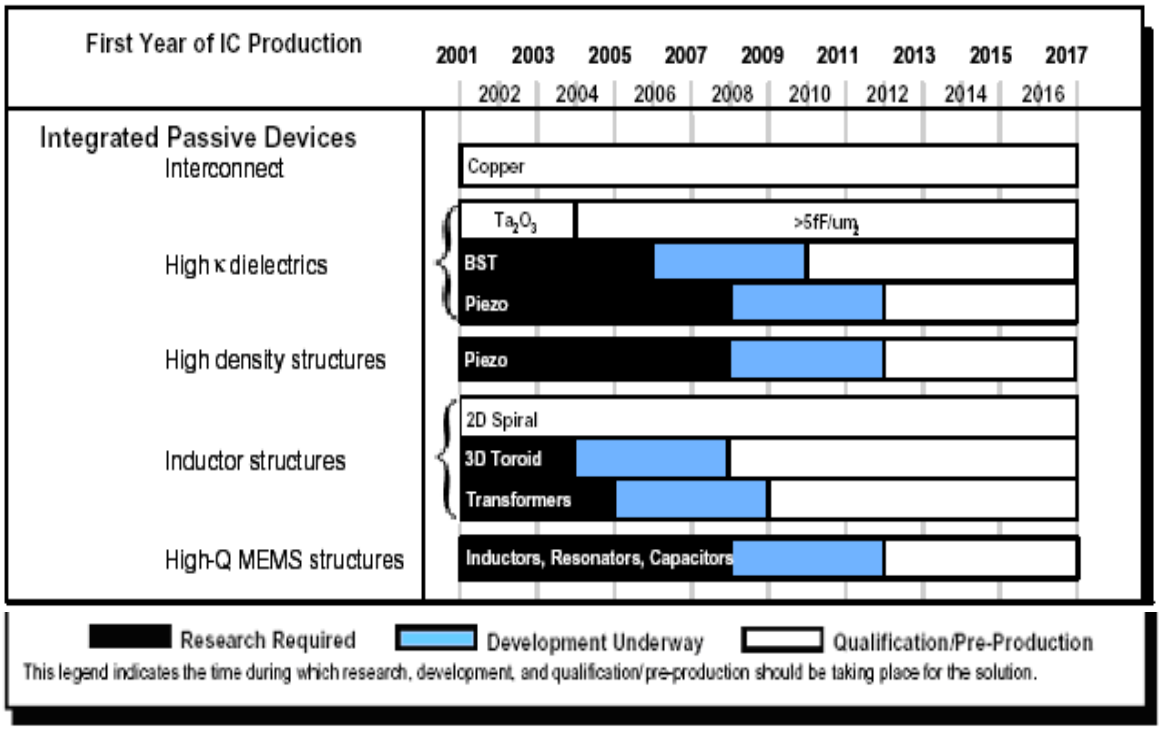



***Figure 1.3.*** *Potential solutions for integrated passive devices provided from The International Technology Roadmap for Semiconductors 2001 [3].*

toroidal/solenoidal, or transformer approaches are available and 3-D counterparts using MEMS technologies are being developed for high-Q and low parasitic performance.

The ITRS is also providing a technology requirement roadmap for transceivers in the frequency range of 0.8-10 GHz. The requirements for RF passives are summarized in Table 1-1 with regard to three circuit blocks: voltage controlled oscillators (VCOs), filters and bypass components, and power amplifiers (PAs). Even though passive requirements vary with application, general requirements can be extracted. For example, Q-factor requirements of inductors are expected to be 10 to 30 in next 15 years. Capacitance density requirements are varying from 0.6 fF/μm$^2$ and 33 fF/μm$^2$ according

to specific applications and time frame. Tunable capacitors used in VCO require their tunability ($C_{max}/C_{min}$) of 3.5 and their Q-factor of 30 to 70.

Examples of tunable capacitor usage in RF wireless applications include tunable band-select filters for wireless communications, phase shifters for electronic scanning of antennas, tunable radiating devices for different frequency selection, and tunable LC circuits for RF impedance matching. Development of low-cost, tunable capacitors will enhance their usage for a variety of commercial and military systems.

Recent research shows nonlinear dielectric, and superconducting perovskite oxide materials such as strontium titanate (STO), barium titanate (BTO), and barium strontium titanate (BST) can be used for high RF performance tunable devices with low-cost, reduced size, and light weight. From the materials science point of view, extensive efforts have been continuously exerted to understand the tuning and loss mechanism in various materials at high frequencies, and improve the material quality. From the RF device implementation point of view, new devices are continuously reported; however, further efforts for advanced architectural improvements of tunable capacitors are still required. For example, in a tunable device using electric field for tuning, a conventionally narrow gap architecture can be used for large tuning at low tuning voltage; however, the narrow gap device is susceptible to undesirable self-modulation effects when the input RF signal is in the range of the tuning bias level. To reduce this intermodulation effect while simultaneously maintaining low tuning voltage, a new architecture is required. Also, an architecture for a compact LC module can be obtained by combination of a tunable capacitor with an inductor.

**Table 1-1.** 0.8-10GHz transceiver technology requirements [3]

| | Year | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2012 | 2015 | 2018 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VCO | Inductor | | | | | | | | | | |
| | Q (5GHz) | 15 | 16 | 17 | 19 | 20 | 22 | 24 | 26 | 28 | 30 |
| | Varactor | | | | | | | | | | |
| | Tuning* | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 |
| | Q (5GHz) | 30 | 32 | 35 | 38 | 41 | 44 | 48 | 52 | 60 | 70 |
| Filter or Bypass | Capacitor | | | | | | | | | | |
| | Density [fF/$\mu m^2$] | 5 | 7 | 9 | 12 | 15 | 19 | 23 | 27 | 30 | 33 |
| | Q (5GHz) | >50 | >50 | >50 | >50 | >50 | >50 | >50 | >50 | >50 | |
| Power Amp. | III-V passives | | | | | | | | | | |
| | Ind. Q | 15 | 15 | 15 | 25 | 25 | 25 | 25 | 30 | 30 | 30 |
| | Cap. Q | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 |
| | By C Den [fF/$\mu m^2$]# | 0.6 | 0.6 | 0.6 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RF C Den [fF/$\mu m^2$]## | 0.6 | 0.6 | 0.6 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Si/SiGe passives | | | | | | | | | | |
| | Ind. Q | 10 | 10 | 10 | 14 | 14 | 14 | 14 | 18 | 18 | 18 |
| | Cap. Q | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 | >100 |
| | By C Den [fF/$\mu m^2$]# | 2 | 4 | 4 | 20 | 20 | 30 | 30 | 40 | 40 | 40 |
| | RF C Den [fF/$\mu m^2$]## | 2 | 4 | 4 | 6 | 6 | 8 | 8 | 10 | 20 | 20 |

*Tuning is defined as $C_{max}/C_{min}$.

# By C Den stands for bypass capacitor density, where bypass capacitor connected between $V_{dd}$ (or $V_{cc}$) and ground. Capacitor breakdown voltage must be rated for appropriate power amplification function.

##RF C Den stands for RF capacitor density, where capacitor used for all other functions (matching, harmonic filtering, coupling, etc). Capacitor must have adequate breakdown for the given application.

## 1.2. Millimeter Wave Antennas

For the last three decades, substantial progress in millimeter wave antennas has been made for use in a wide range of applications such as radio astronomy, radar, imaging, or communication systems [4, 5]. These antennas include wire antennas (dipoles, monopoles, Yagi-Uda antennas, loops, etc.), patch antennas (microstrips, patch resonators, etc.), aperture antennas (rectangular horns, circular apertures, etc.), reflector antennas (parabolic reflectors, corner reflectors, etc.), and end-fire antennas (Vivaldi, tapered slots etc.) [6]. Advanced millimeter wave systems would benefit from having these radiating elements integrated with transmitting or receiving circuits on the same substrates in a monolithic form; such systems have the advantages of compactness, portability, and low-cost in mass production.

Among the various antenna schemes, a planar printed circuit antenna has been used for monolithic millimeter wave systems as a promising candidate because of its low profile, light weight, conformability, low-cost, and ease of manufacture [7]. However, the patch antennas on thick dielectric substrates suffer from severe degradation of the electrical performance due to surface waves, mutual coupling, and dielectric loss of the substrate. There have been efforts to reduce substrate effects, including thinning the substrates [8, 9], and building very thin dielectric layers [10].

On the other hand, while non-planar structures must have potential usage in millimeter wave applications, vertical implementation of those structures has not been massively reported yet. This is due in part because the integrable fabrication of such nonplanar devices is not easy and not cost-effective due to lengthy fabrication steps or

assembly requirements. If an easy and efficient way for 3-D millimeter wave structure fabrication is established, it would provide an alternative to the planar surface patch type antenna or at least give additional degrees of freedom in designing and implementing the millimeter wave antennas. For example, a monopole antenna vertically standing on the substrate suffers less from substrate modes when compared to patch antennas since it is radiating the electromagnetic wave directly through the air. Dipoles or microstrips lifted from the substrate could be accomplished with 3-D fabrication technology, by which no or reduced substrate interaction or loss is involved. Great potential is expected with 3-D fabrication technology in millimeter wave or terahertz systems.

## 1.3. Objectives

This research focuses on the development of advanced architectures and MEMS fabrication technologies for the realization of advanced passive elements for compact RF systems. The objectives of this research are carried out by means of three research vehicles: integrable RF inductors, integrable variable capacitors, and integrable millimeter wave antennas.

The first objective is to develop high-Q, reduced-substrate-dependence, integrable RF inductors. A solenoid type architecture is adopted, by which magnetic coupling to the substrate, leading to eddy current loss could be reduced compared to the conventional spiral type since the magnetic flux of the solenoid geometry is parallel to the substrate. Therefore, it has little interaction with the substrate compared to the spiral inductor, in which the flux is directed perpendicular to the substrate, resulting in large interaction and

resultant eddy current loss. Fabrication technologies for 3-D solenoid structures are developed. Feasibility and usefulness of developed fabrication schemes will be verified by fabricating and testing devices. Also, integration of these structures with CMOS circuitry is discussed.

The second is to develop high performance tunable RF capacitors from the viewpoints of the tunability, high-Q, and suppression of intermodulation distortion (IMD) inherent in tuning devices using nonlinear characteristics. Barium strontium titanate (BST) is employed as a dielectric material because of its high dielectric constant and its electric field dependent permittivity. A fabrication technique for high-Q gap capacitors and a reduced IMD architecture are developed. Concepts and architectures are verified with device fabrication and tests.

The third is to develop 3-D integrable millimeter wave radiating structures by which integrable, less-substrate-dependent antennas can be achieved. In addition, the developed 3-D structure fabrication technology is adding another degree of freedom for designing and fabricating millimeter wave and terahertz radiating systems, as most current integrated antennas are still limited to low-profile planar patch antennas. Feasibility and usefulness is verified with a simple integrable monopole antenna fabrication and its tests.

## 1.4. Outline

This thesis consists of a total of six chapters including this introduction chapter. In Chapter 2, RF passive components reported by other researchers are reviewed; such components include RF inductors, RF capacitors (and variable capacitors), and

micromachined millimeter wave structures. Chapter 3 describes fabrication technologies developed for 3-D structures. These include embedded conductors in polymer, polymer core conductors, reverse-side exposure technique through a transparent substrate, a multi-exposure technique, and inclined patterning. Chapter 4 discusses two of the major architectures developed in this thesis. One is an architecture which enables intermodulation distortion (IMD) reduction in ferroelectric tunable RF capacitors. The other is a compact tunable LC module. Chapter 5 shows six applications of RF components implemented by the techniques developed in previous chapters. These applications include two inductors, embedded inductors and high-aspect-ratio inductors using epoxy core conductors; two tunable capacitors, ferroelectric gap capacitors with low-loss conductors and reduced IMD capacitors; tunable LC resonators; and a W-band monopole antenna. The thesis is concluded in Chapter 6 with a summary and discussion of future work. The overall thesis structure, where related technologies and applications are indicated by arrows, is depicted in Figure 1.4.

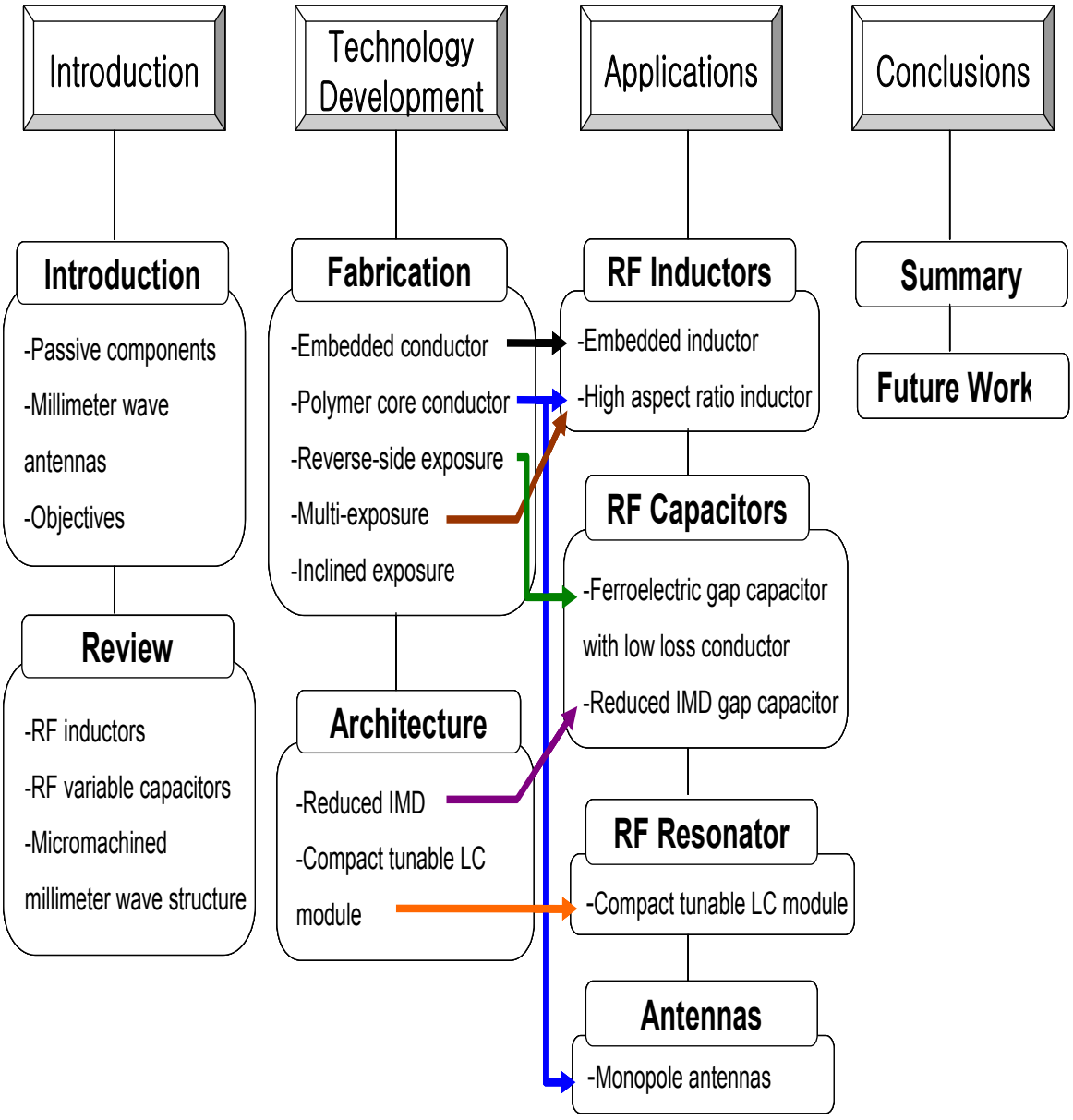



***Figure 1.4.*** *Overview of thesis structure.*

# CHAPTER II

# REVIEW OF RF PASSIVES

## 2.1. RF Inductors

In general, there are two on-chip inductor architectures which have been widely utilized in previous work: a spiral type inductor and a solenoid type inductor. Early investigation of fabricating large spiral inductors on silicon substrates in the ’60s [11] led to the conclusion that poor performance at high frequency (due to large parasitic capacitances limiting its self-resonance frequency and large substrate loss which lowers its Q-factor because of spreading substrate resistance) would preclude their use. Interest in spiral inductors was revitalized when semi-insulating GaAs substrates, which have lower loss at high frequency, began to be used in high frequency applications [12, 13].

While GaAs substrates have been extensively used for RF circuits for several decades, they are expensive compared to silicon, thereby inducing researchers to consider cost-effective alternatives. Recent advances in silicon IC technology enabled its use in the high-frequency application, while maintaining its low-cost merits and advanced digital circuitry development. However, these lossier substrates required the use of new

techniques for integrated inductors to be successful. Substrate coupling and loss could be reduced with the help of a thick oxide isolation process and relatively small coupling area from reduced metal pitch and width.

In the early ’90s, Nguyen et al. reported on-chip spiral inductors with an inductance of 10 nH and a Q-factor of 3~8 in the range of 1 GHz for LC passive filters using a silicon bipolar process as shown in Figure 2.1a [14]. Craninckx et al. reported a hollow spiral at 1.8GHz for a CMOS VCO application [15]. Yue et al. reported Q-factor improvement of a spiral inductor with a patterned ground shield inserted between the inductor and silicon substrate to reduce substrate coupling and eddy current loss in standard CMOS processes as shown in Figure 2.1c [16]. In some cases, for improved inductor performance, spiral inductors based on silicon IC processes were accompanied by bulk substrate etching in Figure 2.1b [17, 18], geometry optimization [19], thick add-on isolation with copper metallization [20], or the introduction of a large air gap between inductor and substrate in Figure 2.1d [21]. The goal was to reduce its substrate effects, which led to a Q-factor in the range of 10 to 25 in the low GHz range.

Integrated solenoid inductors, a differing geometry, were not researched until the mid-’90s, even though most conventional macro-scale magnetic components were solenoid type inductors and the theories related to the solenoid structure were well-developed. A major reason for its not being used earlier is that a solenoid type inductor is a three-dimensional (3-D) structure and it was not easy to implement with conventional integrated circuit techniques. However, with improvements in microelectromechanical systems (MEMS) fabrication technology, 3-D structures can be realized more easily.

Therefore, in the past few years, great advances in integrated solenoid inductors have been observed.

Kim and Allen reported a surface micromachined solenoid inductor with an air core for RF applications in 1998 in Figure 2.2a [22]. The highest Q-factor was approximately 60 on an alumina substrate. Yoon et al. reported surface micromachined solenoid

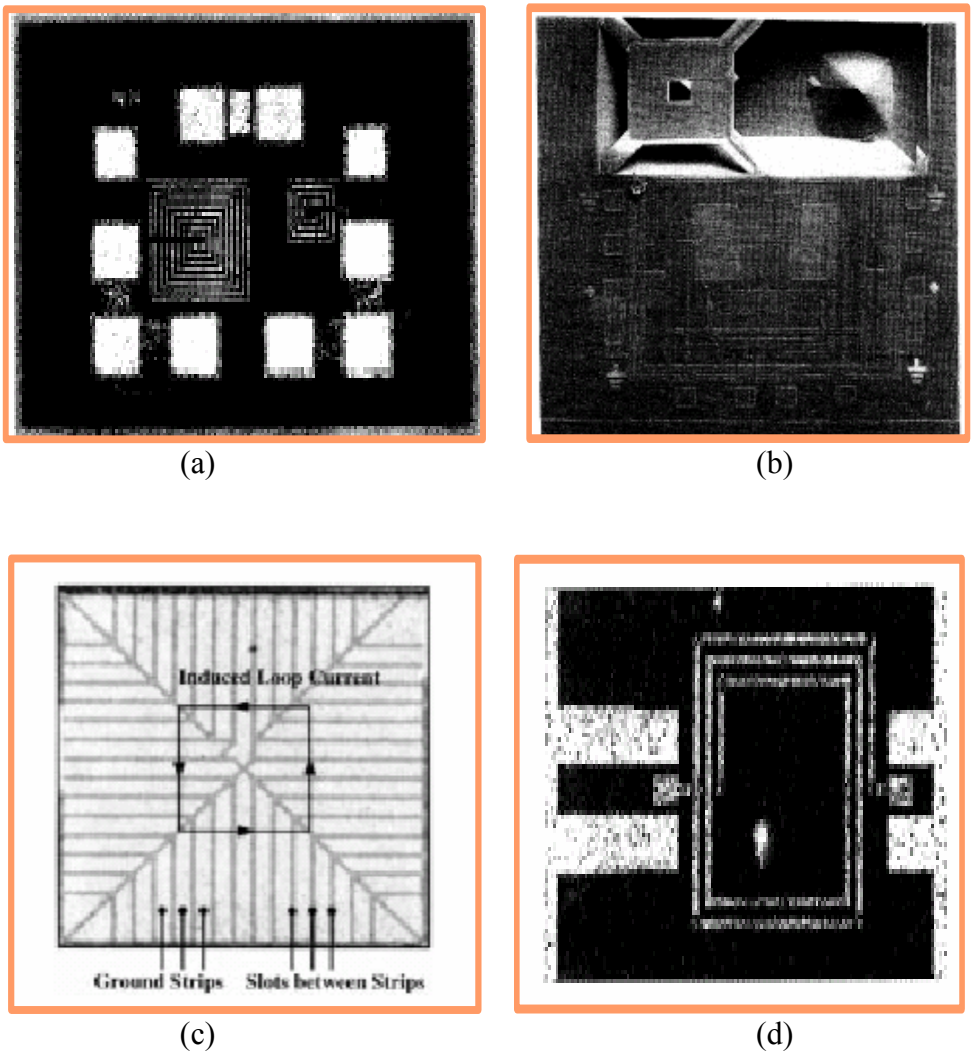



***Figure 2.1.*** *Integrated spiral inductors: (a) On-chip spiral inductor, Nguyen et al. UC Berkeley, 1990 [14]; (b) Silicon substrate bulk etching, Chang et al. UCLA, 1993 [17]; (c) Patterned ground shield, Yue et al. Stanford, 1998 [16]; (d) Large air gap spiral inductor, Park et al. Georgia Tech, 1999 [21].*

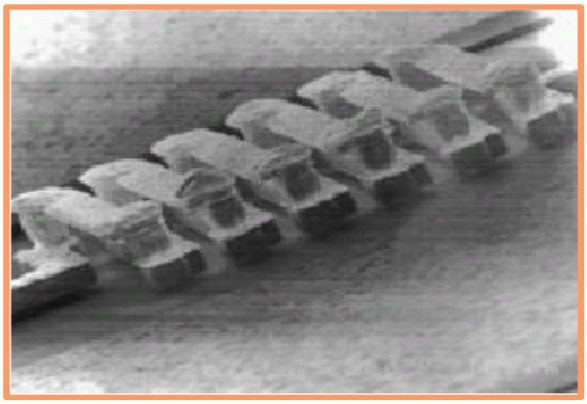
inductors on silicon and on glass with a Q-factor of 16.7 and 25.1, respectively in Figure 2.2b [23]. Joung et al. demonstrated a high aspect ratio solenoid type inductor using an electroplating bonding technique on a printed wiring board (PWB) and reported a Q-factor of 70 in Figure 2.2c [24]. The integrated solenoid approaches with high RF performance, and with less sensitivity to the substrates on which they are fabricated are considered as a very promising approaches for integrated RF inductors.

There were other more exotic approaches to obtain high Q inductors, such as pop-up inductors, which are fabricated in-plane as spiral inductors and erected using magnetic force [25] or surface tension [26] to reduce substrate effects, and a self-assembled out-of-plane inductor using a stress-engineered thin film [27].

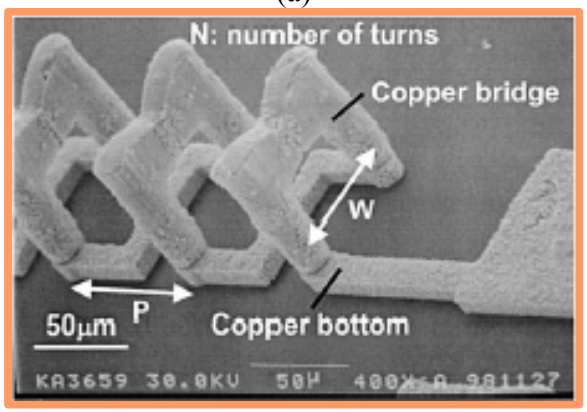
Major integrated inductors and their key properties are summarized in Table 2-1.

**Table 2-1.** Summary of integrated inductors

| | Ref. number | Q-factor | Inductance [nH] | Frequency [GHz] | Substrate | Features |
|---|---|---|---|---|---|---|
| Spiral Inductors | [14] | 3~8 | 10 | 1 | Si | Silicon bipolar process |
| | [15] | 5.7 | 3.2 | 1.8 | Si | CMOS, pattern optimized |
| | [16] | 6~8 | | 1~2 | Si | Patterned ground shield |
| | [17] | | | | Si | Bulk silicon etching |
| | [18] | 17 | 35 | 1.5 | Si | Substrate etching |
| | [19] | 18.5 | 10 | | Si | Geometry optimization |
| | [20] | 24 | 3 | 2 | Si | Cu/SiLK$^{TM}$ process |
| | [21] | 14~18 | 10~25 | 0.1 | Si | 60μm air gap |
| Solenoid Inductors | [22] | 7~60 | 1~20 | 1~10 | Alumin a | 50μm air gap, air core |
| | [23] | 16.7<br>25.1 | 2.67<br>2.3 | 2.4<br>8.4 | Si<br>Glass | 15μm insulating layer |
| | [24] | 70 | | 2 | PWB | Electroplating bonding |
| Miscell-aneous | [25] | | | | | Plastic deformation magnetic assembly |
| | [26] | 20 | 2.0 | 3 | Si | Self-assembly |
| | [27] | 70<br>40 | 8~14<br>6~10 | 1<br>1 | Glass<br>Si | Stress-engineered thin film process |



(a)




(b)

(c)

***Figure 2.2.*** *Integrated solenoid inductors: (a) Solenoid inductor air gap between the substrate and the coil, Kim et al. Georgia Tech, 1998 [22]; (b) Solenoid inductor on Si, Yoon et al. KAIST Korea, 1999 [23]; (c) Solenoid using electroplating bonding technique, Joung et al. Georgia Tech, 2002 [24].*

## 2.2. Tunable RF Capacitors

Electrically tunable capacitors in the microwave frequency range have been under development for more than 60 years. Their development was greatly enhanced by the advent of solid-state devices initiated by the discovery of the bipolar junction transistor in 1948 [28, 29]. Afterward, the solid-state varactor diode was predominantly used in radio frequency integrated circuit (RFIC) applications as shown in Figure 2.3a [30, 31]. While the varactor diode is a mature technology, it suffers from relatively high loss in the RF frequency range and junction noise resulting from electron/hole collisions [32]. In addition, its power handling capability is quite limited because of its low breakdown voltage. The disadvantages of the diode varactor have spurred the appearance of alternative variable capacitor technologies during the last decade. One promising technology is a ferroelectric thin-film variable capacitor.

Among the various ferroelectric materials, barium strontium titanate (BST: $Ba_{1-x}Sr_xTiO_3$) is one of the more popular materials for RF varactors as well as for DRAM capacitors [33]. In particular, thin-film BST has several attractive properties for RF applications [34, 35]. First, BST has an electric-field-dependent permittivity; thus, it can be used as a voltage tunable capacitor, which can be applied to various microwave devices, such as voltage-controlled oscillators (VCO), tunable filters, phase shifters [36], frequency multipliers, and mixers, as shown in Figure 2.3b. Second, it has a high dielectric constant at room temperature and is useful for a highly integrated memory capacitor, a small-area bypass capacitor, or a dielectric layer for MEMS switches. Third, it exhibits high breakdown voltage (typically $3\times10^6$V/cm) and presents a large power

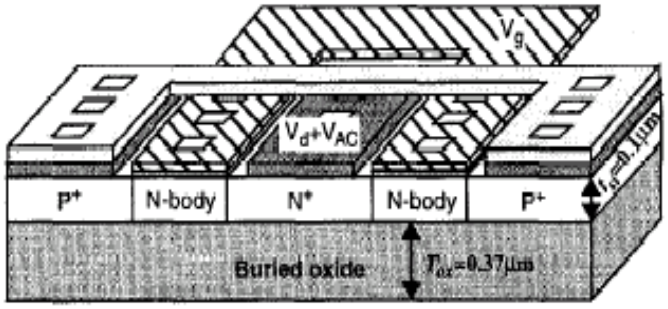
handling capability for RF applications. Extended properties include its fast field response, potentially low dielectric loss, and low fabrication cost. For these reasons, BST-based tunable capacitors have been extensively investigated in order to take advantage of these superior performance characteristics.

Another type of variable capacitor using MEMS technology has also been reported for RF applications as shown in Figure 2.3c [37 - 40]. While a MEMS variable capacitor typically shows high Q-factor (low RF loss), good power handling capability, and good intermodulation distortion (IMD) property, it also exhibits undesirable features such as a need for high control voltage, slow tuning speed, and usually a requirement for vacuum packaging. York et al. compared three competitive variable capacitor technologies for microwave and mm-wave circuits: a GaAs based diode varactor, a thin film BST variable capacitor, and a MEMS variable capacitor [35]. The results are shown in Table 2-2.

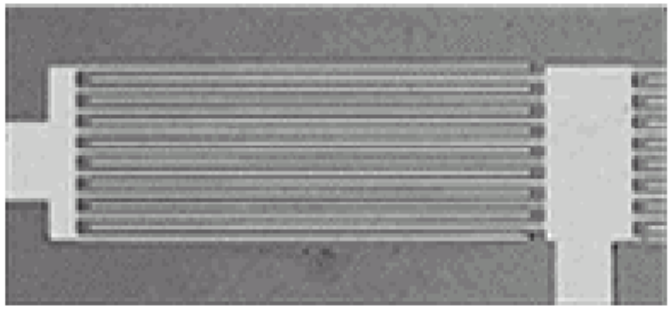
**Table 2-2.** Comparison of varactor technologies for microwave and mm-wave circuits [35]

| | GaAs | BST | MEMS |
|---|---|---|---|
| Tunability (at high Q) | High (4:1 typical) | Moderate (2-3:1) | Low (<1.5:1) |
| RF Loss (Q) | Moderate (Q<60 typ) | Moderate(Q<30 current) | Very Good (Q<200) |
| Control Voltage | <20V (unipolar) | 10-20V (bipolar) | 50-100V (bipolar) |
| Tuning Speed | Fast | Fast | Slow |
| Power Handling | Poor | Excellent | Excellent |
| IMD | Poor | Poor | Excellent |
| Packaging | Hermetic | ?? | Vacuum |
| Cost | Moderate to High | Low? | Low? |

There are advantages and disadvantages for each technology and thus the choice of technology depends on specific applications. For example, a BST variable capacitor could take advantage of its fast continuous tuning at a low bias voltage for a phase shifter or a delay line. In other cases, the fast capacitive nonlinearity would be suitable for




(a)



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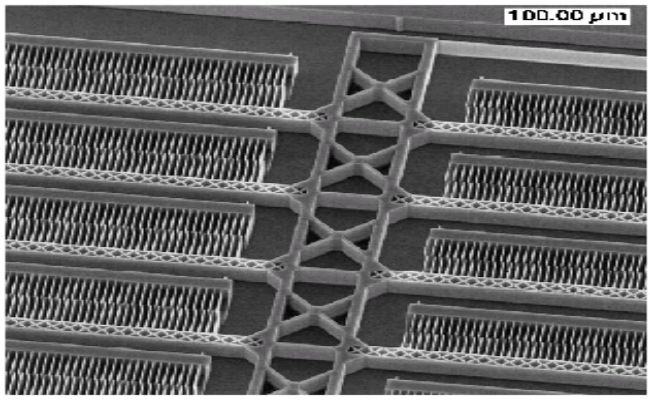



(c)

***Figure 2.3.*** *Variable capacitors: (a) Gate PIN diode on SOI, Hui et al. Hong Kong Univ. , 1998 [31]; (b) BST tunable capacitor on sapphire, Kim et al. Georgia Tech, 2002 [36]; (c) MEMS tunable interdigitated tunable capacitor, Borwick et al. Rockwell Scientific, 2003 [40].*

frequency conversion devices, such as frequency multipliers or upconverters. These applications would not be achieved by relatively slow MEMS variable capacitors. Meanwhile, the nonlinearity for frequency conversion would be a drawback for linear components, such as a phase shifter resulting from intermodulation distortion (IMD). This issue will be discussed later, where an architecture to reduce IMD without losing its tunability at low bias voltage will be proposed. A BST variable capacitor benefits from high power handling capability from its high breakdown voltage, which is not the case with a GaAs varactor. On the other hand, a BST variable capacitor does not seem to be appropriate for high Q-factor applications, such as a narrowband tunable filter or a phase shifter with low loss, at least in current material quality.

The dielectric properties of deposited BST depend on several factors, such as deposition and anneal temperature, composition, crystallinity, film thickness, etc. [41, 42]. Also, there are various deposition methods for thin-film BST, such as RF-sputtering [43], metal organic chemical vapor deposition (MOCVD) [34], combustion chemical vapor deposition (CCVD) [44], sol-gel [45], pulsed laser ablation [46] etc. So far there does not seem to be a standard or best method for thin-film BST forming.

For the variable capacitor applications of thin-film BST, geometrical optimization of electrode patterning as well as optimal material conditions should be determined to achieve high tuning with low electrical loss. A thick metallization process for a narrow gap capacitor for low RF loss and high tunability will be addressed in a later section. Also, a reduced IMD capacitor architecture with the BST variable capacitor will be discussed. Several variable capacitors using different architectures are listed in Table 2-3.

**Table 2-3.** Various tunable capacitors

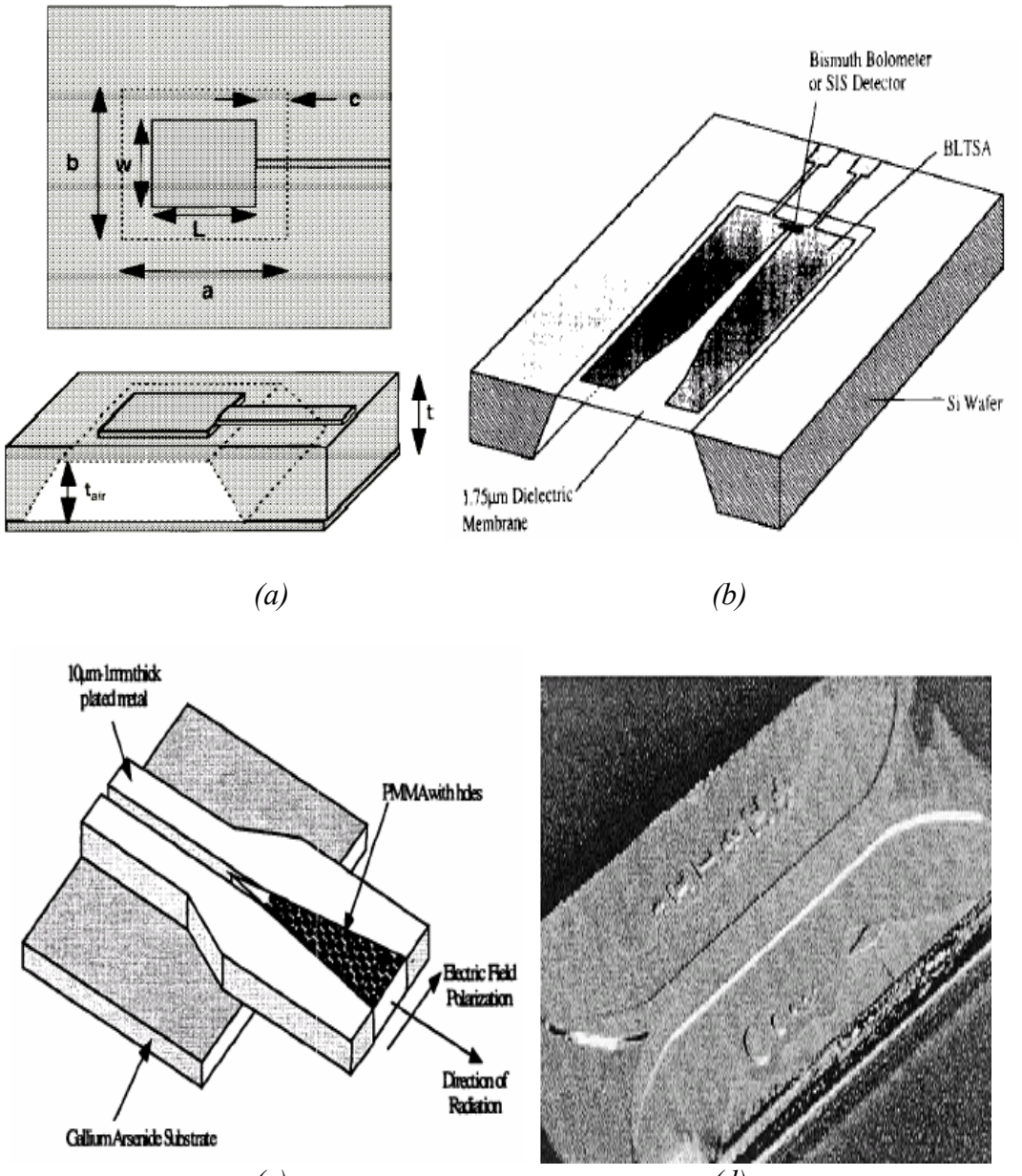
| | Ref. number | Q-factor | Capacitance [pF] | Tunability $C_{max}/C_{min}$ | Frequency [GHz] | Substrate | Architecture | Features |
|---|---|---|---|---|---|---|---|---|
| Diode varactor | [30] | >30 | 1.02 | 11 @10V | 1-10 | GaAs | p-n diode | |
| | [31] | 14 | 7 | 6 @2V | 1 | SOI | Gated PIN diode | CMOS process |
| BST variable capacitor | [34] | 12 | 65 | 3.4 @9V | 0.045-0.5 | Si | parallel cap | $\varepsilon_r$ =100-200 MOCVD |
| | [47] | 10<br>20 | 0.15-2 | 2 @30V<br>2.2@100V | 20<br>10 | glass<br>Sapp. | parallel cap<br>gap cap | RF sputter or MOCVD |
| | [36] | 15-60 | 1-5 | 3.1@140V | 2 | Sapp. | gap cap | CCVD |
| MEMS variable capacitor | [37] | | 0.04-0.08 | 1.7 @18V | 0.045-10 | glass | parallel cap | |
| | [39] | >17 | 1.9-6.7 | 3.5 | 1.5 | Si | multi-finger | |
| | [40] | 100 | 1-5 | 8.4@8V | 0.225-0.4 | Si | Multi-finger | |

## 2.3. Micromachined Millimeter Wave Antennas

Twenty years later after Maxwell [48] formulated his electromagnetic equations, Hertz [49] experimentally verified the wave phenomena using a hertzian dipole. Since then, the dipole and the monopole antennas have been studied and utilized as the most elementary, but useful, antennas [50 - 53]. In millimeter wave applications, the dipole antennas and other microstrip antennas are implemented and analyzed as a planar printed circuit type on a dielectric substrate because of its low fabrication cost and ease of manufacture at the cost of electrical performance degradations due to surface waves or mutual coupling [54 - 56]. Much effort has been exerted to reduce the surface wave effects using micromachining processes, which includes suspending patch antennas on thin dielectric layers or close-spaced periodic holes [57, 58] and patch antennas on thinned substrates as shown in Figure 2.4a [59]. End-fire type antennas also have taken advantage of micromachining approaches. A linearly tapered slot antenna built on a thin dielectric layer has been reported [60] as shown in Figure 2.4b and a tapered slot antenna (TSA) fabricated using LIGA process combined with complete removal of part of the substrate has also been demonstrated [61] as shown in Figure 2.4c. As a waveguide type antenna, a horn antenna fabricated using a thick photolithography step has been reported [62] as shown in Figure 2.4d. However, the height of the structure is not sufficient to provide efficient performance such as might be expected from an antenna which is a quarter-wavelength or half-wavelength in height.

The nominal vertical dimension required for millimeter wave applications is in the range of a few hundred micrometers to a few millimeters. Integrable and efficient fabrication techniques for these tall structures are quite challenging, and satisfactory

vertical implementation examples have not been widely reported yet. Efficient fabrication technology to achieve those tall structures will be discussed in the following chapter and an implementation example will be introduced.




*(a)* *(b)*

*(c)* *(d)*

***Figure 2.4.*** *Micromachined millimeter wave antennas: (a) Micromachined patch antennas having air cavity underneath patch antenna [59]; (b) Broken LTSA antenna integrated on a thin dielectric membrane [60]; (c) LIGA TSA with PMMA dielectric loading [61]; (d) Micromachined waveguide with horn antenna [62].*

# CHAPTER III

# DEVELOPMENT OF FABRICATION TECHNIQUES FOR 3-D STRUCTURES

The development of surface micromachined 3-D solenoid type inductors is a major portion of this research. As a starting point, much effort has been expended in the development of 3-D electrical conductors. Several techniques for complicated 3-D polymer structures and 3-D conductors are developed. These developed 3-D conductors are not only applied to the integrated inductor but also directly extended to much higher frequency applications such as integrated millimeter wave antennas. In fact, increase in operation frequency reduces the appropriate radiator size, which meets the dimensions feasible for the developed 3-D conductor technologies. These generic fabrication technologies are expected to contribute to a broad frequency range of RF applications.

## 3.1. Embedded Conductors in Polymer

Metal vias are used for layer-to-layer electrical contacts in both the IC and MEMS industries. It becomes higher-aspect-ratio (height to width ratio) because the isolating

dielectric layers become thick to reduce capacitive coupling or other parasitics while the via width becomes narrow to increase integration density. It is imperative to develop an efficient fabrication process for interconnecting conductors.

For the IC industry, IBM introduced the DAMASCENE process for multi-layer interconnects using copper electroforming through an oxide mold [63]. Conformal copper electrodeposition along with an uneven surface was performed, leaving an excess grown copper over the entire surface. This excess copper was finally removed by a chemical mechanical polishing (CMP) process. The oxide layers were intended to remain at the end of the process by which the process time was shortened and the remaining oxide layers provided mechanical stability to withstand later harsh packaging processes such as an injection molding process.

In the MEMS area, high-aspect-ratio via fabrication techniques using UV lithography and plate-through-mold were applied to various electromechanical parts, such as gears [64], magnets [65], and RF inductors [22, 23]. In the plate-through-mold approach, the plating time is lengthened proportionally to the depth of the mold to fill. In addition, the mold is required to be removed after the plating, which prolonged the process time further. Moreover, removal of some polymeric molds such as polyimide or SU-8 often relies on expensive dry etching processes, which is not favorable, especially as the mold becomes thicker.

In some micromachining applications, keeping the mold as a part of device or system is desirable as in the case of vias in IC chips discussed above. Keller et al. reported the HEXSIL process where molded poly silicon and molded metal in poly silicon were implemented using deeply etched silicon molds and conformal plating to

make micro tweezers or other actuators [66, 67]. They also used lapping and polishing processes to get rid of excess portion of metal or poly silicon. Cros and Allen reported a molded metal process in SU-8 for magnetic-cored spiral coils [68], where polymer was intended to remain after the process as part of the device. They used a conformal plating process but a wet etching step instead of polishing to remove the excess metal portion to avoid possible problems in polishing. For example, if the polishing process wore the excess metal unevenly, the early exposed part could experience further unevenness during polishing due to different mechanical properties of metal and the mold material. In the case of inorganic molds such as oxide or silicon, the mold material is more resistant to the polishing process than metal, thus metal has a little bit of recess in the end. But the recess is usually not significant. However, in the case of an organic mold such as polymer, it is much softer than metal and experiences a much greater recess, often resulting in distortion of the top metal pattern or delamination of the whole polymer layer due to the shear stress during polishing. Thus the chemical wet etching process was used. The etching process, however, contains a potential limit in patterning different-aspect-ratio conductors. The wet etching makes a great recess in the metal portion when the via opening size is large relative to the height. For a successful via process, an aspect ratio greater than 5 was recommended [68].

In this section, another fabrication process for an embedded conductor in polymer is proposed, which is especially suitable for RF passive component fabrication. This embedded conductor fabrication uses an unusual plating technique of two plating processes simultaneously occurring: a conformal plating process through non-removable via mold and a conventional plate-through-mold process through removable upper

conductor mold. This process has several advantages. First, via conductors are embedded in the mold from which they are formed and the mold is not removed after structures are completed. This eliminates a long etching step for the mold removal, which simplifies the process. Also, the electroplating to fill up the via mold is carried out by conformal plating, which does not increase plating time with increased via height. Second, because the conductors are embedded in the mold, the resultant embedded conductor is mechanically strong and robust. This reduces microphonics as well as enables the complete devices out of this technique to survive subsequent electronic packaging processes (such as injection molding or other chip packaging treatments). Third, the fabrication is carried out at temperatures as low as 110°C, which makes it compatible with the CMOS process.

### 3.1.1. Fabrication

The fabrication process of embedded conductors in polymer uses negative tone photosensitive epoxy (SU-8, Microchem, Inc.) for non-removable polymer mold, negative photoresist (NR9-8000, Futurrex, Inc.) for removable polymer mold, and copper (Cu) for electroplating. Figure 3.1 details the fabrication process. An SU-8 epoxy layer (~ few hundred μm) is spin-coated, cured, and patterned for via definition on the substrate (Figure 3.1a). In order to remove residual solvent, the sample is placed in an oven at 60 °C for 10 hours. The sample is then treated with oxygen plasma briefly for approximately one minute. After seed layers (Ti/Cu/Ti, 20nm/200nm/20nm) are deposited using a DC-sputterer, a thick (20μm) negative photoresist NR9-8000 is spin coated (Figure 3.1b). In order to avoid mold damage due to the expansion of air trapped in the via mold, the

sample is baked at lower temperature for a longer time (i.e. 30 °C for 24 hours) instead of at a high temperature for a short period. The mask covering the via and top electrode

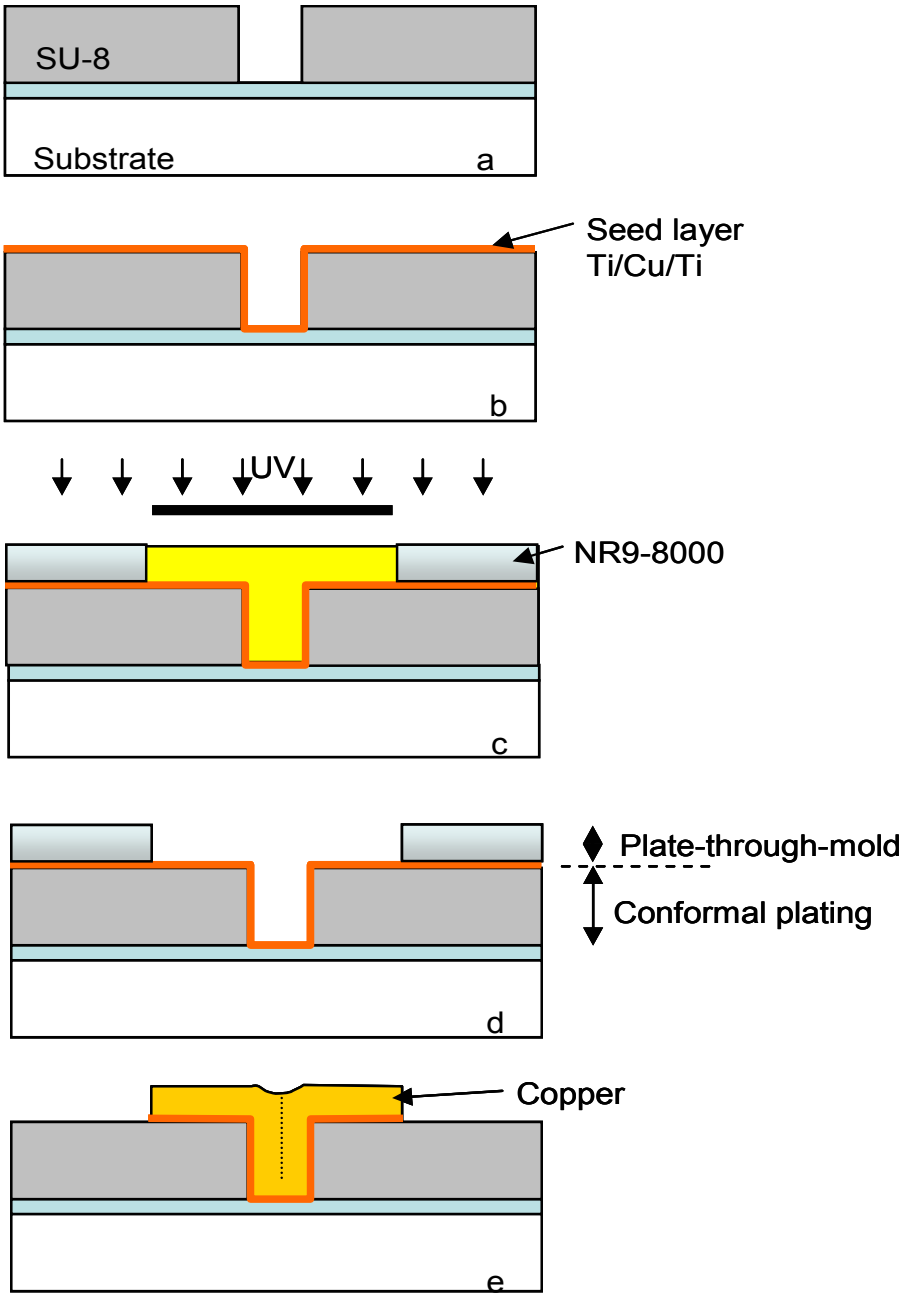


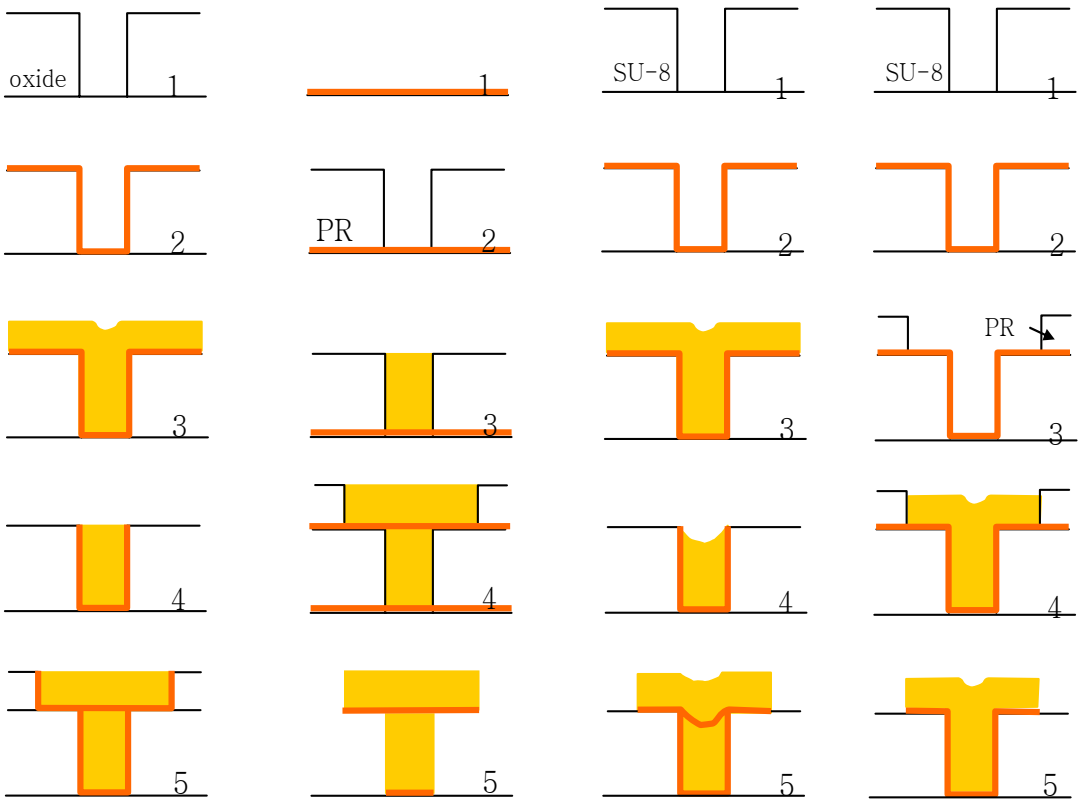

***Figure 3.1.*** *Fabrication process for embedded conductors in polymer.*

pattern is aligned and exposed using UV (Figure 3.1c). Note that we are using negative photoresist and the optical dose for top 20 μm layer is necessary regardless of the via depth. After developing the photoresist, a double layer mold is formed (Figure 3.1d). A single electrodeposition will fill the double layer mold simultaneously with two different schemes: a conformal plating process for the via mold and a conventional plate-through-mold process for the top electrode pattern. After plating, the top photoresist (NR9-8000) is dissolved in acetone and the seed layer is time-etched to complete the process (Figure 3.1e). The SU-8 mold surrounding the via as well as the electroplated Cu structure remains. Note that both the via post and the SU-8 mold mechanically support the structure, which serves as a platform for the next layer process.

As a reference, various processes for via conductor fabrication are summarized in Table 3-1 and fabrication process comparison for one via and one upper conducting layer configuration in Figure 3.2.

**Table 3-1.** Various processes for via conductor fabrication

| | Damascene [63] (Dual-step Damascene) | Conventional plate-through-mold process [22] | Conformal plating process with etch-back [68] | Conformal plating process without etch-back[this work] |
|---|---|---|---|---|
| Mold material | Oxide (ceramic) | Polymer (organic) | Polymer (organic) | Polymer (organic) |
| Mold removal | No | Yes | No | No |
| Metal deposition time | Short | Long | Short | Short |
| Number of plating per two layers | 2 (1) | 2 | 2 | 1 |
| Excess metal removal | Polishing (CMP) | No | Chemical etching | No |
| Mold erosion or metal dishing | Susceptible during CMP | N/A | Metal dishing during etch-back | N/A |
| Metal source usage | Non economical | Economical | Non economical | Economical |
| Device packaging | Injection molding | Polymer or cavity packaging | Injection molding | Injection molding |
| Applications | IC interconnect | RF passives, MEMS actuator, MEMS interconnect | RF passives, MEMS interconnect, Power devices | RF passives, MEMS interconnect, Power devices |




| (a) | (b) | (c) | (d) |
|---|---|---|---|
| *1. Oxide via mold*<br>*2. Conformal seed layer*<br>*3. Conformal electroplating*<br>*4. Polishing*<br>*5. Repeat 1~4* | *1. Seed layer*<br>*2. PR via mold*<br>*3. Plate-through-mold*<br>*4. Repeat 1~3*<br>*5. Remove PR and seed layer* | *1. SU-8 mold*<br>*2. Conformal seed layer*<br>*3. Conformal electroplating*<br>*4. Wet etching*<br>*5. Follow (b)3~5* | *1. SU-8 mold*<br>*2. Conformal seed layer*<br>*3. PR patterning for upper layer*<br>*4.Conformal+plate through mold*<br>*5. Remove PR and seed layer* |

***Figure 3.2.*** *Fabrication process comparison for one via and one upper conducting layer configuration: (a) Damascene process; (b) Conventional plate-through-mold process; (c) Conformal plating process with etch-back; (d) Conformal plating without etch-back.*

### 3.1.2. Fabricated Structures

Figure 3.3 shows a fabricated solenoid type inductor using the process of embedded conductor in SU-8. The optical photomicrograph shows both upper and lower electrodes through transparent SU-8 molds in Figure 3.2a while the SEM image shows only upper electrodes in Figure 3.2b. A schematic of cross-section (A-A') is shown in Figure 3.2c with geometrical dimension noted. The via has approximately a 3:1 aspect-ratio. The structure is lifted by 25 μm from the substrate using the first SU-8 layer to reduce substrate effects such as parasitic capacitance or eddy current loss due to electromagnetic coupling. The probe and ground pads are placed in the upper electrode level to facilitate testing. Performance of this type of embedded inductor will be discussed in Chapter 5.1.1.

### 3.1.3. Discussion

In this embedded conductor process, there exist several difficulties. First, delamination between SU-8 layers and subsequent seed layers (Ti/Cu/Ti) often occurs. It is understood to be due to residual solvent from SU-8 mold. After the SU-8 development step, it is recommended that sufficient time for residual solvent removal be used and an additional flood exposure followed by the post bake step be performed. Second, after the PR is coated for upper conductor patterning, the air trapped in via hole grows during baking and bursts, leading to poor photo patterning. It is recommended to bake the sample in lower temperature for a longer time rather than at a higher temperature for a shorter time, to prevent air bubbles from blowing up. Alternatively, a dry film photoresist

can be used such as Riston (Dupont Co.), by which upper mold patterning can be facilitated. Third, plating within deep trenches or vias suffers from voids or seams in the

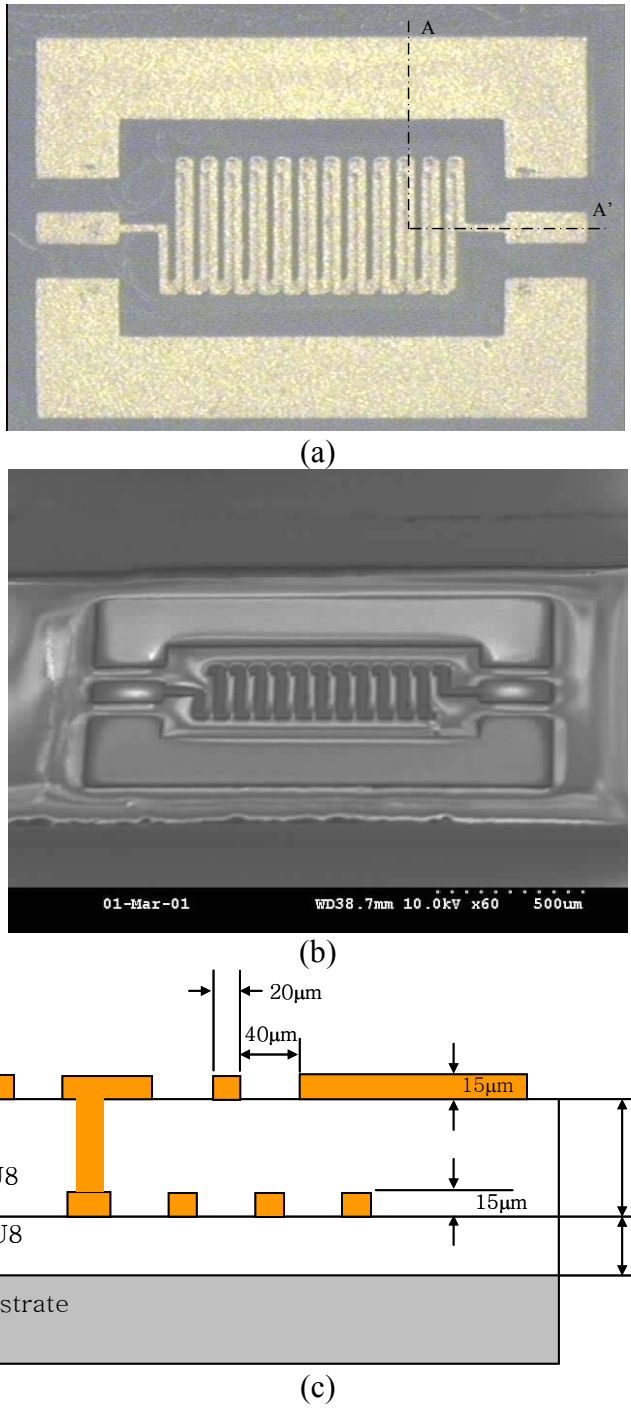



***Figure 3.3.*** *A fabricated solenoid structure using the process of embedded conductor in SU-8: (a) Top view using optical microscope; (b) SEM view; (c) Schematic of cross-section A-A' .*

bottom of the via. The air trapped inside via during plating would prohibit metal to uniformly grow. Degassing from the via can be helped by a vacuum system. The samples can be placed in a beaker with de-ionized (DI) water before plating. The whole beaker is placed in vacuum jar to remove the air trapped in the via. In this experiment, the sample was degassed in 70 mTorr for 30 minutes in DI beaker, with the sample moved relative to the plating solution. In this experiment (via aspect ratio of 3:1) it was not plated in a vacuum environment during plating period, but such vacuum plating would be encouraged for structures with much higher aspect ratio. Non-uniform growth along with the via wall occurs due to unbalanced mass transfer factors such as non-uniform electric field or limited convective flow of plating solution within the deep via. Plating in a weak current density condition associated with low electric field will assuage the non-uniform growth. Various additives or surfactants can be used to obtain uniform plating along with deep vias or trenches. More details regarding plating through deep trench can be reference to Joung's thesis [69].

Various 3-D inductors can be implemented using the embedded conductor approach. 3-D schematics and cross-sectional views of solenoid type, toroid type, spiral type, and meander type devices are shown in Figure 3.4.

The embedding material used here was SU-8, but this approach is not restricted to SU-8. Various polymers (whether photodefinable or not) such as other epoxies, polyimide, poly methyl methacrylate (PMMA), poly dimethylsiloxane (PDMS), benzocyclobutene (BCB), Poly urethane (PU), and others can be used for the mold.

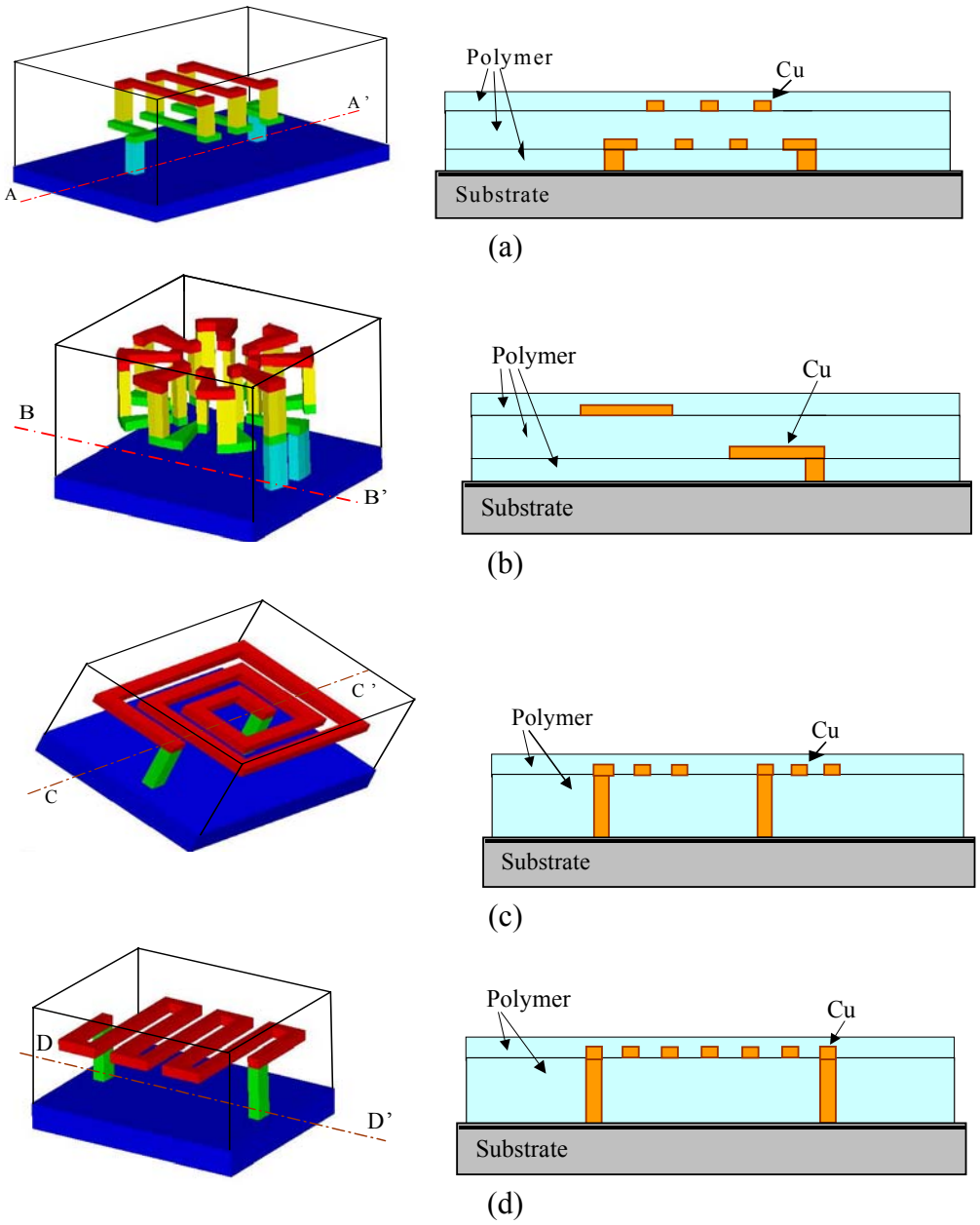



***Figure 3.4.*** *Schematics and cross-section view of various 3-D micromachined inductors: (a) Solenoid-type inductor; (b) Toroid-type inductor; (c) Spiral type inductor; (d) Meander-type inductor.*

The thickness of the polymer layer can be in the range of several μm to several hundred μm. However, the thickness of the polymer layer does not affect the conformal deposition time. Also, this process is low temperature process and compatible with the underlying CMOS processes.

## 3.2. Polymer-Core Conductors

It is well known that as frequency increases, an electromagnetic wave propagating through a good conductor attenuates very quickly in the depth direction of the conductor and the resultant electric current flows through the outermost portion of the conductor. The distance where the electromagnetic wave reduces in amplitude by a factor of 1/e is called the skin depth $\delta$.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad (3.1)$$

where $\omega$ (rad/sec) is the angular frequency of the electromagnetic wave, $\mu$ (H/m) the

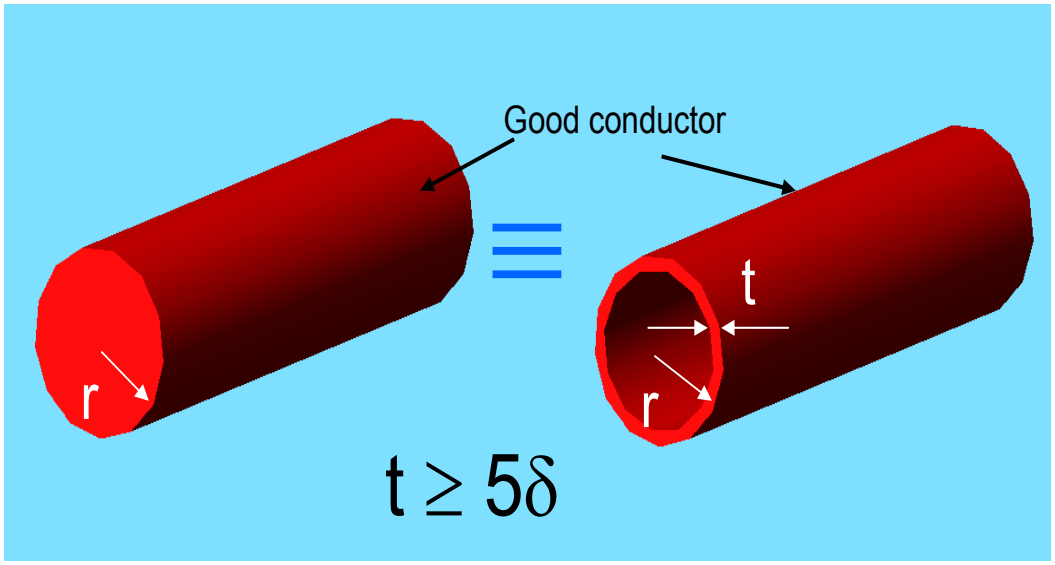



***Figure 3.5.*** *Solid conductor (left) vs. hollow conductor(right) in the high frequency regime.*

permeability of the conductor, and $\sigma$ (S/m) is the electrical conductivity. There is no advantage to construct RF transmission lines or wires with thickness much larger than the skin depth. A hollow conductor whose conductor thickness is greater than a few skin depths is considered electrically equivalent to the solid conductor where outer diameters of both conductors are the same as in Figure 3.5.

A vertical electrical interconnect or a via for RF applications could be fabricated much more efficiently using a hollow shape conductor. Consider two fabrication

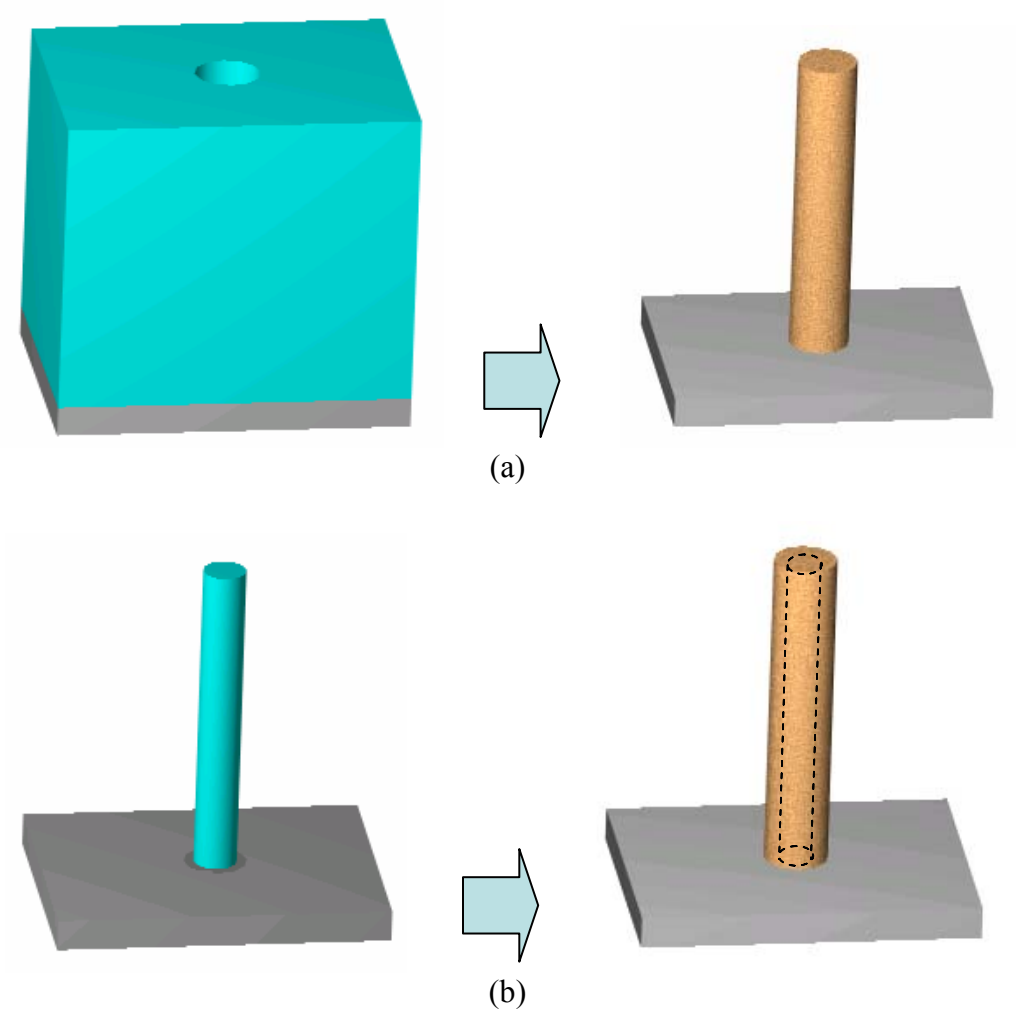



***Figure 3.6.*** *Two approaches for vertical interconnects: (a) Solid conductor; (b) Polymer-core conductor.*

approaches for a high-aspect-ratio interconnect in Figure 3.6. One approach is to make a concave via mold and fill it solidly with plated metal, which will be called a solid conductor process in Figure 3.6a. The other is to make a high-aspect-ratio polymer column and cover it with plated metal, which will be called a polymer core conductor process in Figure 3.6b. For a high-aspect-ratio interconnect, vertical sidewall patterning is important. SU-8 (Microchem, Inc.), a negative tone photodefinable epoxy, is known to give a very good sidewall profile with UV lithography [70, 71]. With SU-8 material, it is relatively easy to fabricate lines or columns of a given aspect ratio as opposed to trenches or vias of the same aspect ratio [72]. In addition, metal electrodeposition on the column surface is much easier than via hole filling to obtain void-free and seamless conductor structures.

In this section, a fabrication process for high-aspect-ratio RF conductors is developed using polymer column patterning and subsequent electrodeposition over the column, by which high-aspect-ratio RF components are realized in a simple and efficient fashion when compared to conventional approaches. More importantly, the concept of the polymer-core conductor (or in this case epoxy-core conductor) combining epoxy backbone patterning with subsequent metallization provide a methodology for obtaining relatively easily complex 3-D shapes of various RF components by taking advantage of advanced 3-D epoxy fabrication technologies. The developed polymer core conductor technique will be applied to fabricate RF passive components such as inductors as well as millimeter wave radiating components in later chapters.

### 3.2.1. Fabrication Process

The fabrication process is described in Figure 3.7. It shows two metal steps: one for bottom conductor patterning and the other for vertical epoxy core conductor patterning.

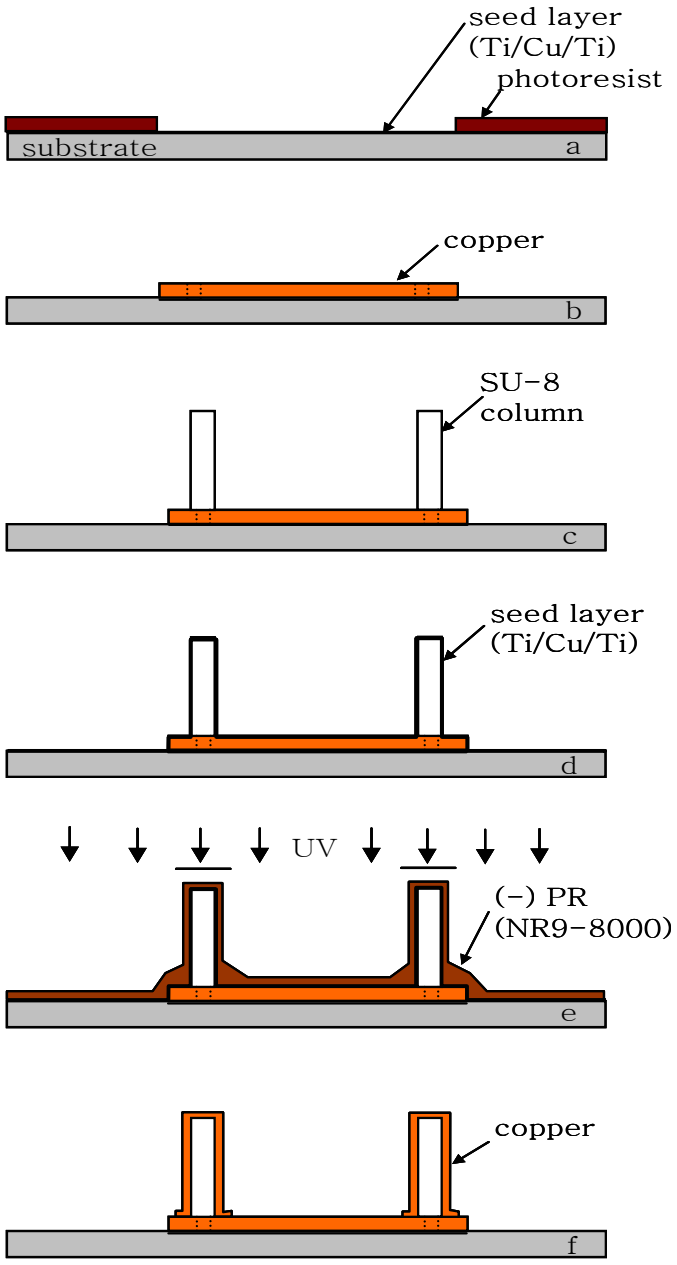



***Figure 3.7.*** *Fabrication process using a proximity patterning scheme for the column metallization.*

First, a bottom seed layer (Ti/Cu/Ti, 20 nm / 200 nm / 20 nm) is deposited on a substrate using a DC sputterer. A 20 μm thickness of photoresist AZ 4620 (Clariant Co.) is spin coated and patterned for the bottom conductor (a). Copper electroplating is carried out and the PR and the seed layer are removed (b). A single SU-8 layer is coated to a thickness ranging (depending on the application) of several micrometers to millimeters, where the thickness of the SU-8 becomes the height of the vertical conductor (c). A conformal seed layer (Ti/Cu/Ti, 20 nm / 500 nm / 20 nm) is deposited using a DC sputterer (d). Thin negative-tone photoresist, NR9-8000 (Futurrex, Inc.), is spin coated, where an excess of the viscous photoresist is observed to build up at the corner of the column and the bottom layer due to surface tension of the photoresist. This thicker portion at the corner potentially causes poor patterning. A proximity photolithography is performed for the column patterning on this uneven surface (e). The negative tone photoresist is useful in this patterning because a small amount of optical dose for the thin bottom layer crosslinking is sufficient with negative resist, while a positive tone photoresist would need a much larger optical dose to dissolve the portion of resist covering the tall column. After conformal electroplating, the photoresist and the seed layer are removed sequentially to complete the process (f).

Figure 3.8 shows successfully fabricated epoxy core conductors. Figure 3.8a shows an SEM image of 200 μm tall and 100 μm wide SU-8 columns on bottom conductors. Figure 3.8b is an optical photomicrograph of the top view of the columns after proximity photolithography of the mold for selective column plating. Figure 3.8c and 3.8d are showing an SEM image of a complete epoxy core conductor array and a magnified one, respectively. The thickness of bottom conductors and column-covering conductors are 15

μm and 20 μm, respectively. The final height and width of the epoxy core conductor are 235 μm and 140 μm, respectively.

Figure 3.9 shows an example of unsuccessful conductors. 200 μm tall and 50 μm wide columns are nicely patterned on bottom conductors (Figure 3.9a). Due to the surface tension of the viscous photoresist between closely placed columns, a curtain shape of

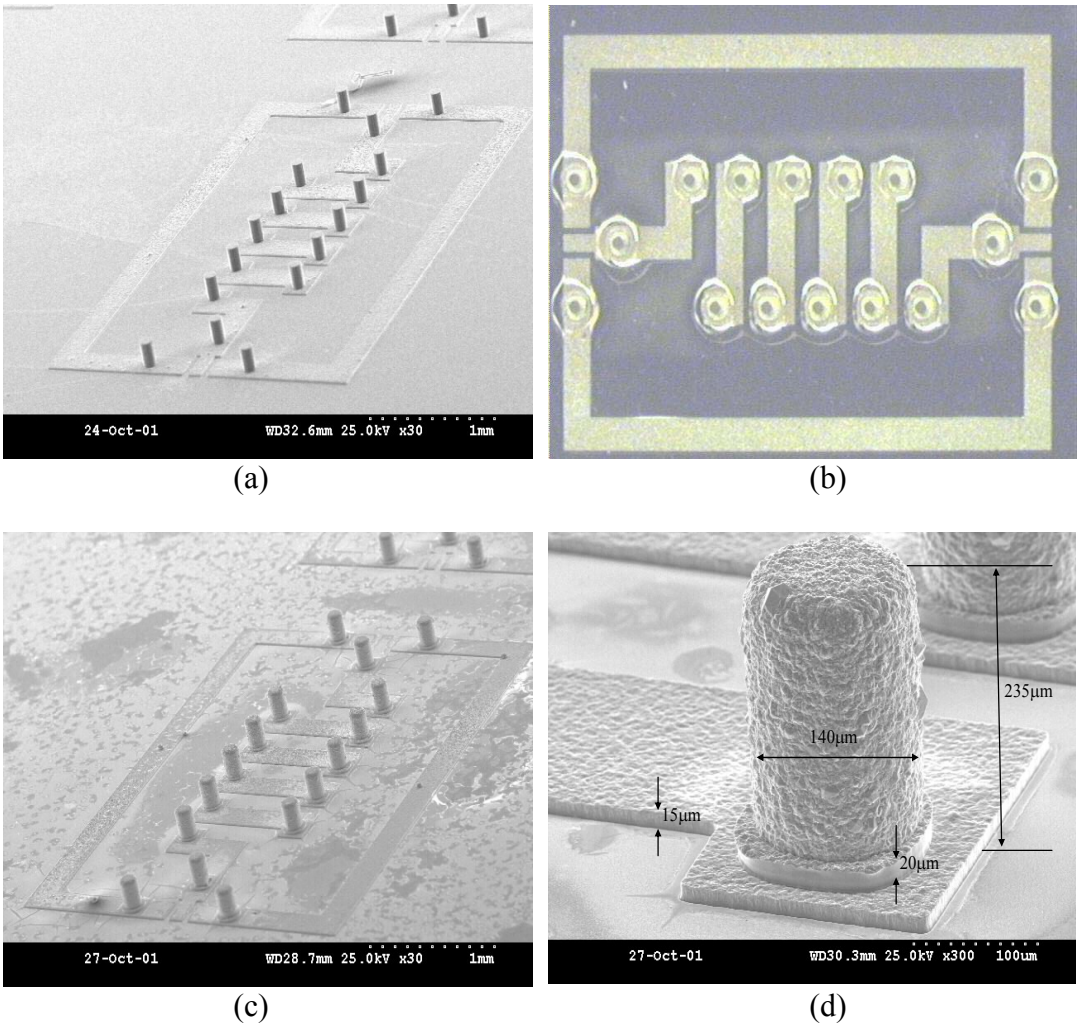



***Figure 3.8.*** *Successfully fabricated epoxy-core conductor: (a) SU-8 column patterned on bottom electrodes (Figure 3.7d); (b) Top view of column patterning using proximity lithography (after Figure 3.7e); (c) Complete epoxy-core conductors (Figure 3.7f); (d) A magnified single epoxy core conductor.*

photoresist profile is formed between the columns as shown in Figure 3.9b. The resultant epoxy core conductor is shown in Figure 3.9c with discontinuous conductors. The magnified viewgraph is shown in Figure 3.9d. One fourth of the column is not covered with electroplated copper.

One way to prevent this kind of discontinuous patterning from occurring is to use a

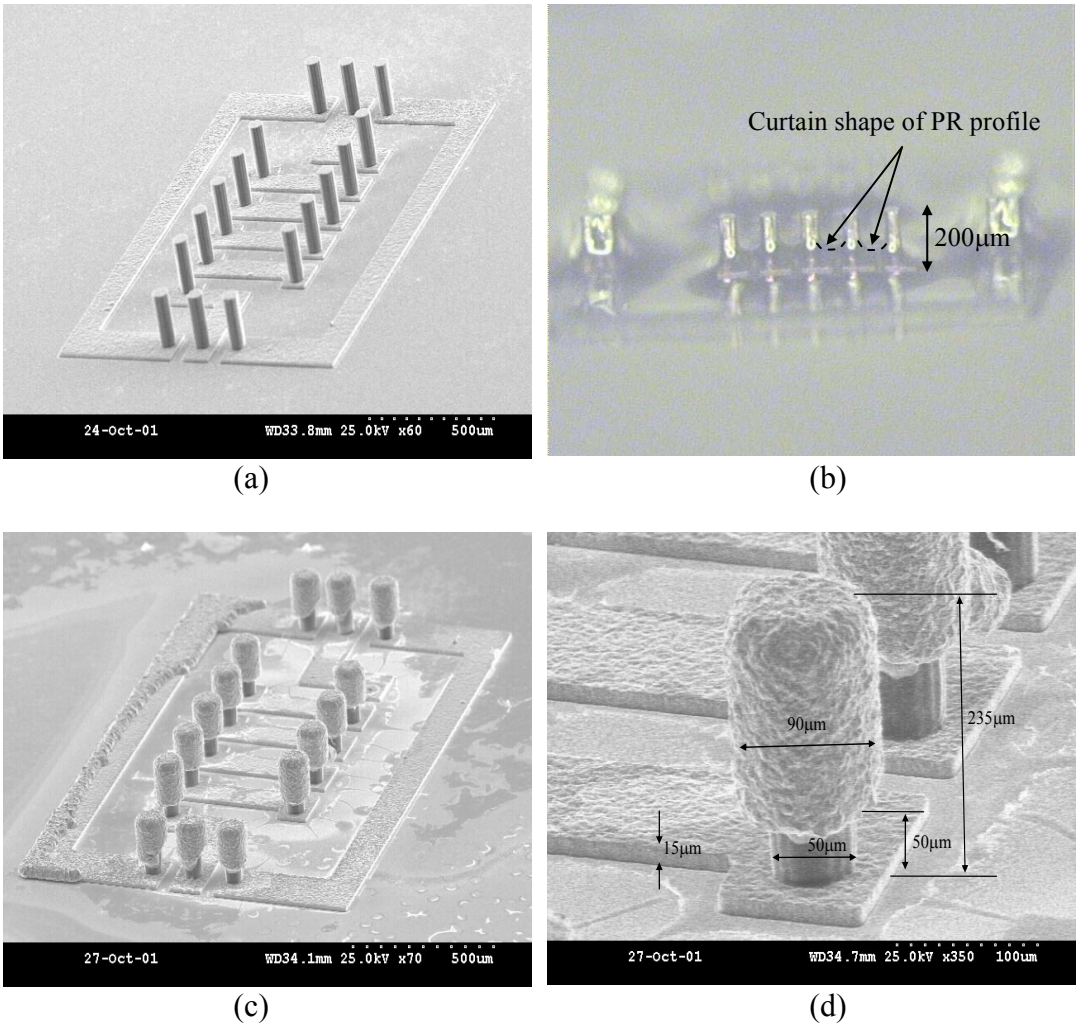



***Figure 3.9.*** *Unsuccessfully fabricated epoxy-core conductor: (a) SU-8 column patterned on bottom electrodes (Figure 3.7d); (b) Side view of columns after photoresist coating for proximity photolithography (Figure 3.7e); (c) Complete epoxy-core conductors (Figure 3.7f); (d) A magnified single epoxy core conductor.*

multi-coating technique with less viscous photoresist to minimize the curtain-shape PR profile. Alternatively, a pre-patterned seed layer scheme for the column metallization can be used. Figure 3.10 details the process. First the three differently-functioning layers are deposited in sequence: a seed layer (Cr/Au; 20 nm / 150 nm), a passivation layer (SiO2; 1 μm or thin SU-8; 2 μm), and a sacrificial layer (Ti/Cu; 20 nm / 1 μm) (a). Patterning for the bottom conductors are performed using copper and titanium etching followed by oxide or SU-8 etching (b). Tall SU-8 column is patterned (c). Another seed layer (Cr/Au, 20 nm /150 nm) is conformally deposited using a DC sputterer (d). The sacrificial copper layer is etched using cupric sulfate saturated ammonium hydroxide solution. In this step, Cr/Au on top of copper is also lifted off. Titanium is etched using diluted hydrofluoric acid (HF) etchant (e). Copper and gold are plated up to thicknesses of 15 μm and 1 μm, respectively. The top gold is used for a protection layer during subsequent seed layer etching and as an anti-erosion final layer for the RF components. The remaining passivation layer and the seed layer are removed to complete the process (f).

Figure 3.11 shows a pair of epoxy core conductors simultaneously fabricated with a bottom conductor using a pre-patterned seed layer scheme. Since the vertical conductors and the horizontal conductor are monolithically fabricated by a single electroplating step, they do not have an intermediate layer between each part, resulting in potentially improved mechanical and electrical properties compared with the previous structure. In addition, closely placed vertical conductors (pitch between columns: 200 μm, column height: 300 μm) in this process are successfully fabricated, as opposed to the disconnected failed conductors (pitch between columns: 200 μm, column height: 200 μm) observed in the previous process and shown in Figure 3.9.

For the selective metallization of the epoxy core, two methods were discussed. There is the possibility for direct metallization of epoxy column using electroless plating with use of a conductive epoxy or surface treatment. Although this could result in fabrication

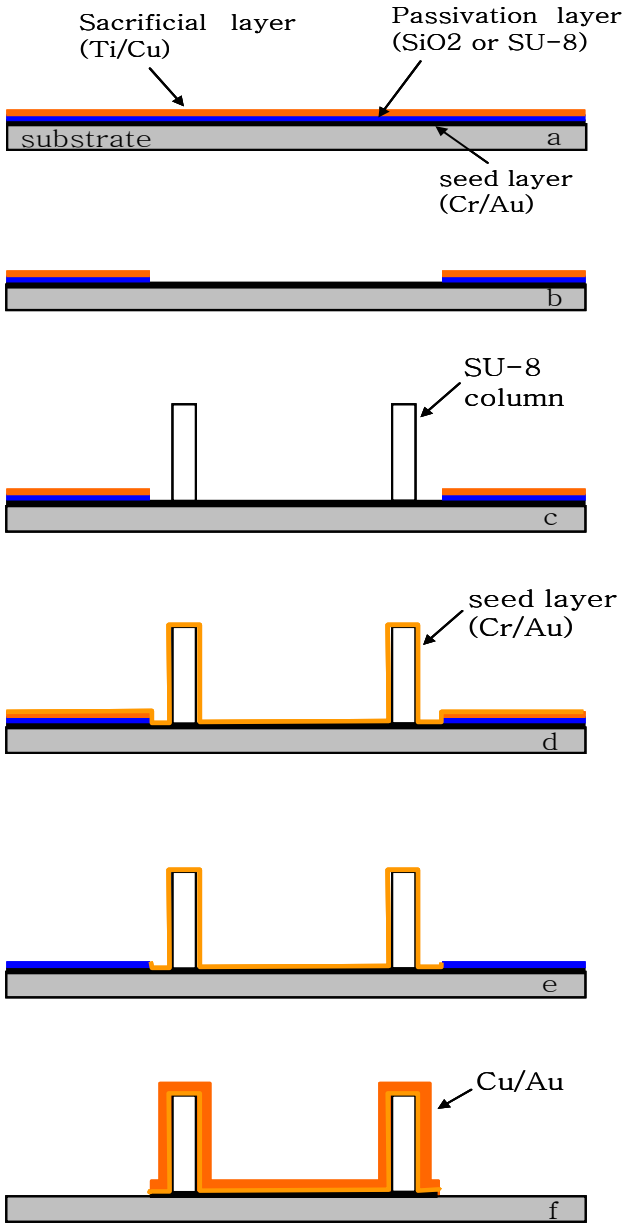



***Figure 3.10.*** *Fabrication process using a pre-patterned seed layer scheme for the column metallization.*

simplification, it was not extensively researched here.

The solid conductor and polymer core conductor fabrication schemes are summarized in Table 3-2.

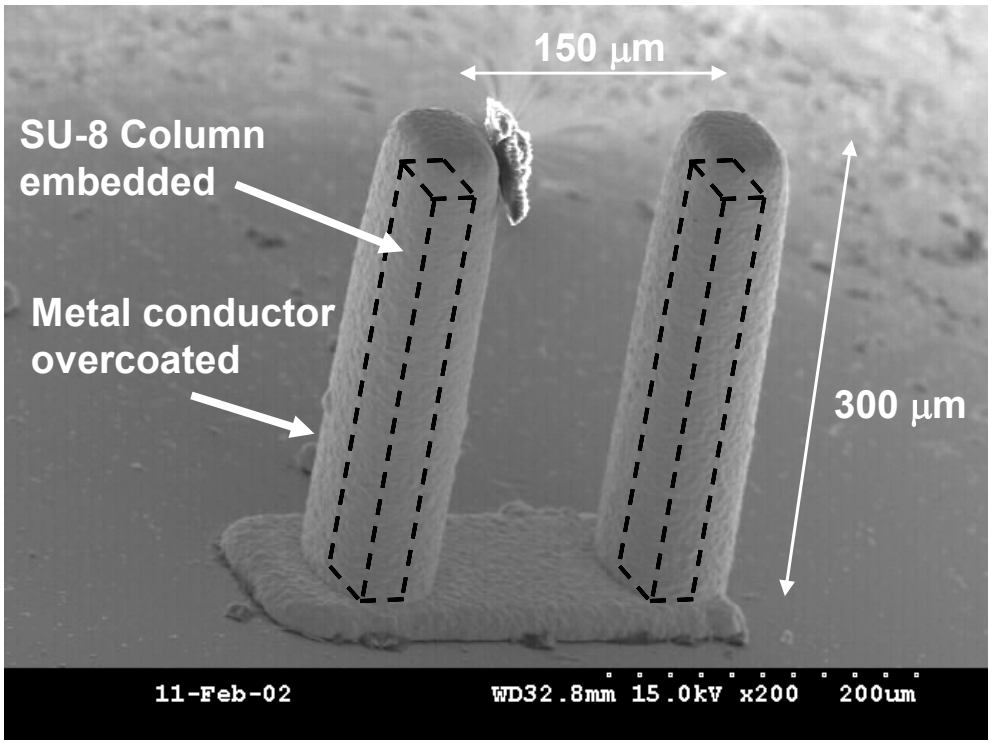



***Figure 3.11.*** *Epoxy-core conductor fabricated using a pre-patterned seed layer scheme for the column metallization.*

**Table 3-2.** Process comparison of *solid conductor* process and *polymer-core conductor* process using UV lithography and plating

| | Solid conductor process | Polymer core conductor process |
|---|---|---|
| Conductor type | Solid | Hollow |
| Polymer structure | Via mold | Column |
| High-aspect-ratio patterning material | SU-8: moderate - difficult | SU-8: moderate |
| Reasonable aspect ratio | ~5 | ~10 |
| Metallization | Via filling plating (difficult)<br>-stirring<br>-vacuuming<br>-additives | Column coating plating (easy)<br>-mild stirring |
| Plating time | Long~ medium | short |
| Mold removal | Required; solvent or dry ashing | No |
| Photolithography | Single mold patterning | Column patterning and Selective metallization (proximity UV lithography, pre-patterning, or electroless plating) |
| Preferred applications | High Power MEMS conductor | RF MEMS; 3-D inductors, transformer, vertical coaxial interconnect, millimeter wave antennas |

## 3.3. Reverse-side Exposure through Transparent Substrate

MEMS or microelectronic devices can utilize various materials as substrates. Some materials such as Si, GaAs, alumina, metals etc. are opaque to the UV light source while others, such as glass, quartz, sapphire etc. are transparent to it. When optically transparent substrates are employed, additional flexibility in photolithographic-based patterning is enabled. For example, appropriate optical doses can be applied not only from the upper- (front-)side, but also from the reverse- (back-) side, as shown in Figure 3.12. In this section, useful applications of the reverse-side exposure through transparent substrates are discussed in three subsections: fabrication of a high-aspect-ratio structure, a self-alignment scheme, and the usage of substrate optics.

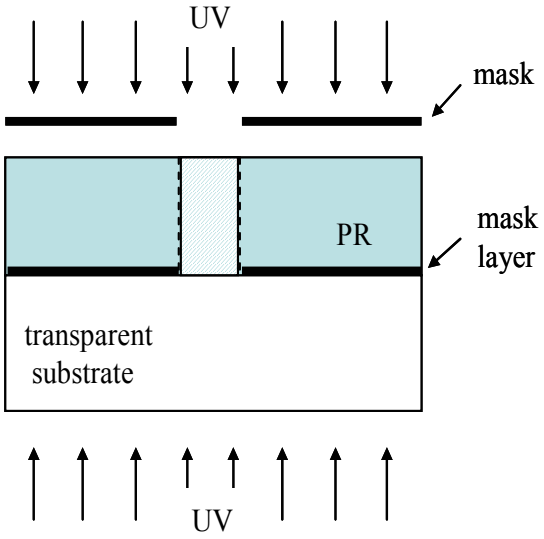



***Figure 3.12.*** *Exposure flexibility with transparent substrate: Both upper- (front-) side exposure and reverse- (back-) side exposure are available.*

### 3.3.1. Fabrication of High-Aspect-Ratio Structure

SU-8, a negative tone photodefinable epoxy is used for UV-based high-aspect-ratio patterning. The fabrication sequence for the reverse-side exposure is shown in Figure 3.13. A thin masking metal layer (usually 200nm of Cr) is deposited and patterned on the transparent glass substrate (a). Thick SU-8 is applied on the substrate, followed by UV exposure through the substrate mask layer (b). In practice, the sample is turned over and placed under a regular UV source with light incident from the top. A high-aspect-ratio structure is obtained after development (c). The mask layer can either be removed or

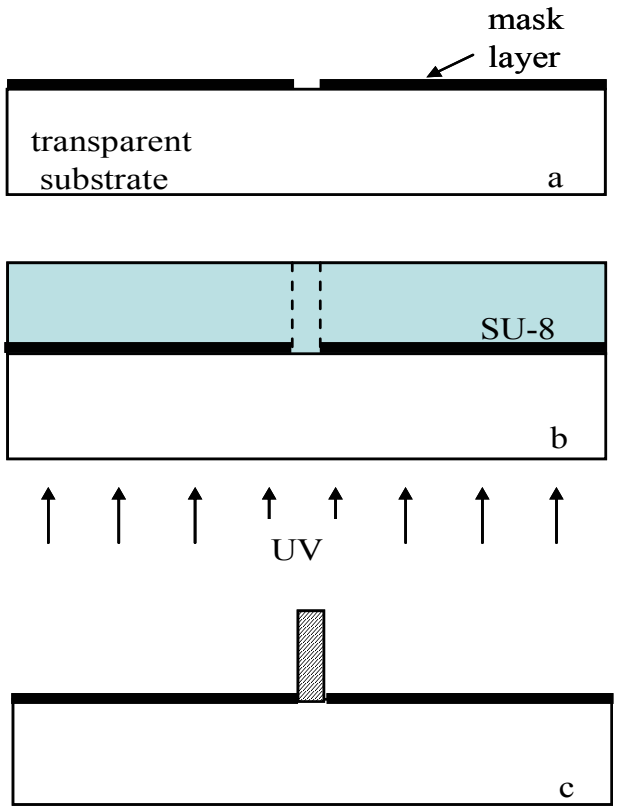



***Figure 3.13.*** *Fabrication approach for reverse-side exposure of high-aspect-ratio column.*

allowed to remain depending on the requirements of the subsequent steps.

This approach provides several advantageous features compared to the front-side exposure for high-aspect-ratio fabrication. First, a secure contact between the photo mask layer and the polymer layer is guaranteed regardless of surface roughness or edge-bead formation during or after a polymer coating step, thereby allowing a sharp pattern to be obtained. (This is because in contact photolithography, poor contact causes the diffraction of light at the edge of an opaque feature in the mask, potentially resulting in blurred or diffused pattern edges.) Figure 3.14 shows high-aspect-ratio column structures fabricated with the good contact resulting from backside exposure, an optimized optical dose, and an optimized development condition. Aspect ratio exceeding 13:1 (diameter to height) has been achieved.

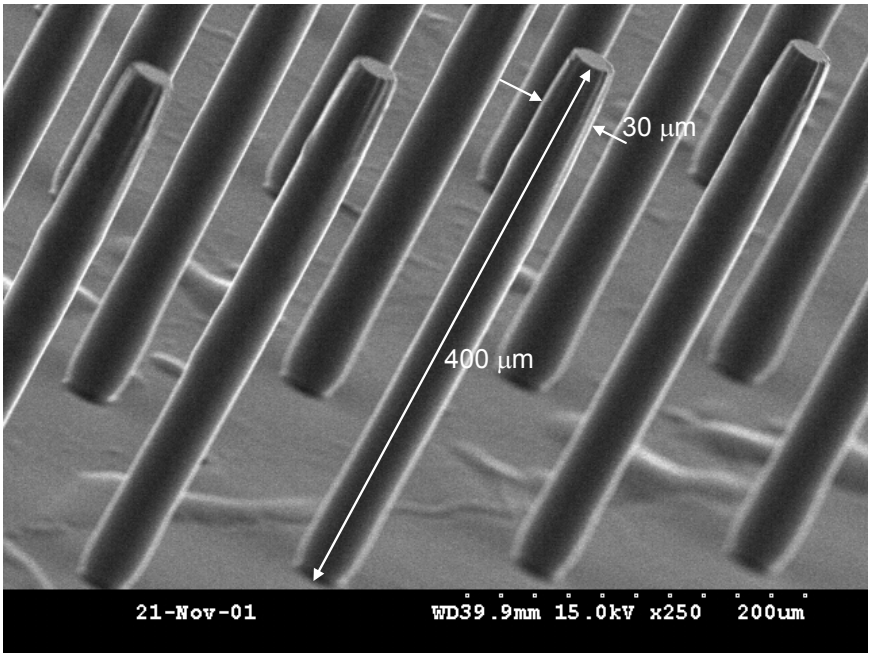
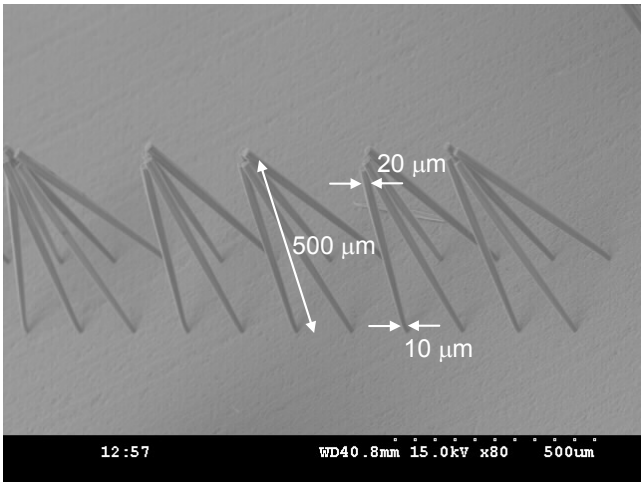
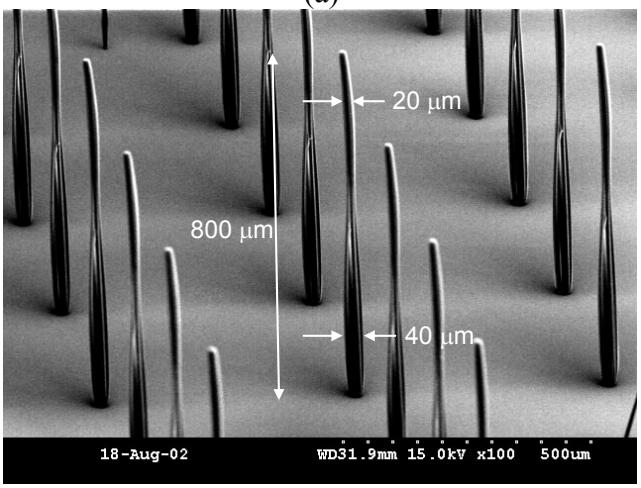



***Figure 3.14.*** *High-aspect-ratio column structure with good mask contact (ensured through backside exposure) combined with optimized optical dose and optimized development conditions.*

Using the reverse-side exposure scheme, additional optical dose is absorbed in the bottom portion of the column, resulting in a strong mechanical structure in the lower portion of the column. Figure 3.15 shows fabricated tall column structures using (a) a regular front-side exposure and (b) a reverse-side exposure. Figure 3.15a shows the diameter of the top portion of the column is 20 μm while that of the lower portion is 10 μm, thinner due to lack of optical dose. The height is 500 μm. The structures are




(a)




(b)

***Figure 3.15.*** *Fabricated high-aspect-ratio column structures using (a) Front-side exposure and (b) Reverse-side exposure.*

mechanically weak in the lower portion, leaning over toward others in their group during the drying process due to solvent surface tension. In contrast, the columns fabricated from the reverse side exposure are nicely standing up to 800 μm tall as shown in Figure 3.15b. The diameter of the bottom portion is 40 μm while that of the top portion is 20 μm. Mechanically strong column structures are obtained from the reverse-side exposure and an aspect ratio of more than 20:1 has been achieved.

### 3.3.2. Self-alignment Scheme

Reverse-side exposure can be applied to narrowly-spaced thick electrode fabrication on a transparent substrate, where a standard lift-off process is used for metallization. For

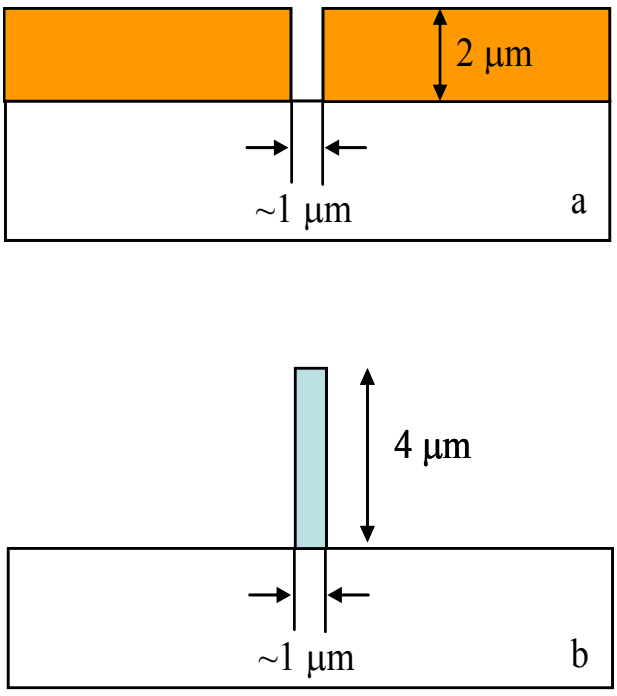



***Figure 3.16.*** *Thick electrodes with narrow gap: (a) Electrodes with the gap of 1 μm and the thickness of 2 μm; (b) Required mold for the lift-off process with a width of 1 μm and a height of 4 μm.*

example, assume it is desired to fabricate two electrodes of thickness 2μm with a gap of 1 μm as shown in Figure 3.16a. The photoresist mold for the lift-off process should be thicker than the ultimate conductor, resulting in a high-aspect-ratio mold as shown in Figure 3.16b. The thick metal lift-off process using a high-aspect-ratio mold often experiences failure for at least two reasons: the difficulty of high-aspect-ratio mold fabrication and the metal step coverage during the long deposition period. In order to avoid the high-aspect-ratio process, a repeated, multistep lift-off process can be performed using a low-aspect-ratio mold and a thin electrode deposition to ultimately obtain the final desired thickness at the cost of multiple alignment and exposure. Figure 3.17 shows the fabrication process. Metal patterning (1 μm thick) is performed using a relatively thin mold and a lift-off process (a). Thicker negative tone photoresist is coated and the reverse-side exposure is performed using the previous metal layer as a photomask, where no mask alignment is necessary, i.e. self-alignment is accomplished (b). In addition, the resultant mold adheres securely to the substrate after development since the contact area between the mold and the substrate increases as much as the side wall of the first metal layer (c). A second lift-off is performed to obtain thicker electrodes (d). An additional metal layer can be added by repeating the steps b-d if necessary. Note that this approach eliminates the alignment step which would otherwise be necessary in a conventional repetitive lift-off approach

This scheme has been utilized to implement a narrowly spaced low-loss conductor for a ferroelectric gap capacitor on a sapphire substrate [73]. The details are discussed in Chapter 5.2.1.

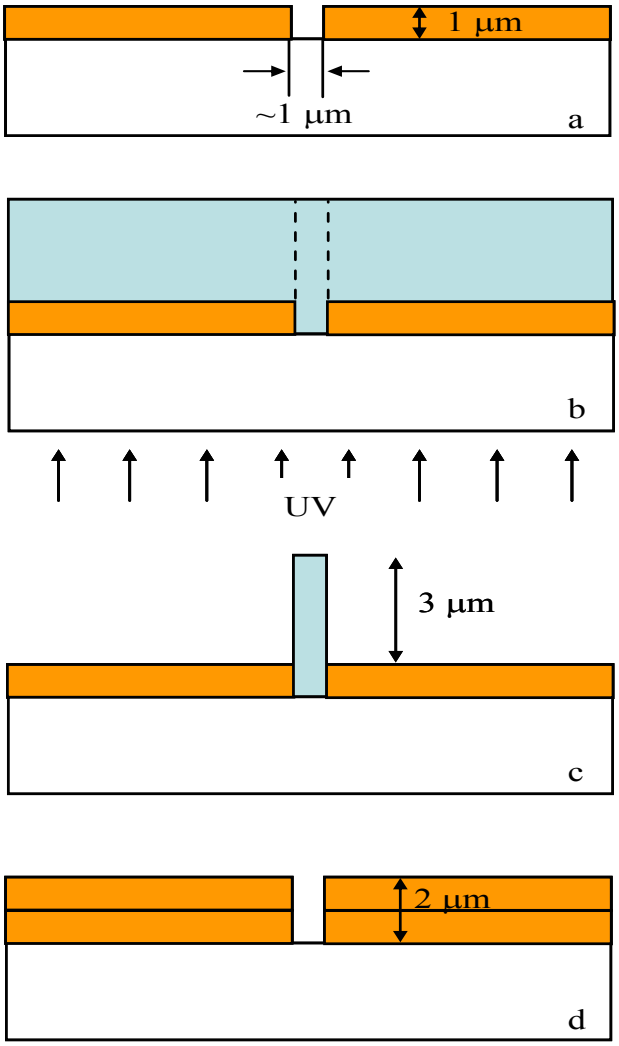


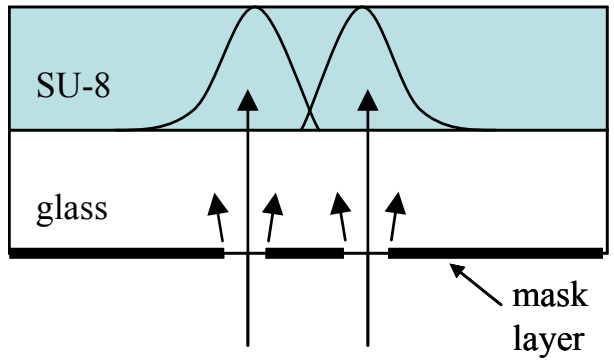

***Figure 3.17.*** *Fabrication process for thick electrodes with a narrow gap using a repeatable self-alignment reverse-side exposure technique.*

### 3.3.3. Usage of Substrate Optics

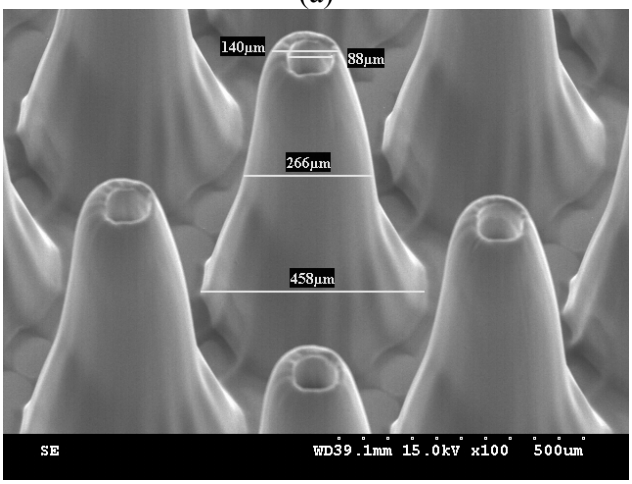
Various unusual patterns can be generated by the combination of reverse-side exposure and modified substrates. This effect has been exploited in this work as well as by others. For example, placement of a metal mask layer on the other side of the

substrate as shown in Figure 3.18a gives an unusual pattern. Incident light first meets the mask pattern and is diffracted at the edge of the opaque mask pattern. The diffracted light has a large lateral deviation from the non-diffracted light after its passage through the 1.5 mm thick glass substrate. The light is then refracted at the interface of the glass substrate and the SU-8 layer due to the difference of their refractive indices. The resultant SU-8 patterns with a concentric circle mask of an inner diameter of 100 μm and an outer diameter of 200 μm is shown in Figure 3.18b.

Polymer coating on a substrate with isotropically etched concave patterns produces




(a)




(a)

***Figure 3.18.*** *Patterning with the mask layer placed in the outer surface of the substrate: (a) Schematic of the exposure scheme; (b) Resultant structure.*

integrated lens functionality at the interface due to their refractive index differences. High-aspect-ratio tapered structures were fabricated as shown in Figure 3.19 [74]. While these structures were used for a microneedle application, they could also be applied to RF applications such as a tapered monopole antenna fabrication.

Unitary polymer substrate and column structures were implemented using flood exposure with low UV dose through the transparent substrate [75]. The exposure scheme and a fabricated structure are shown in Figure 3.20a and b, respectively.

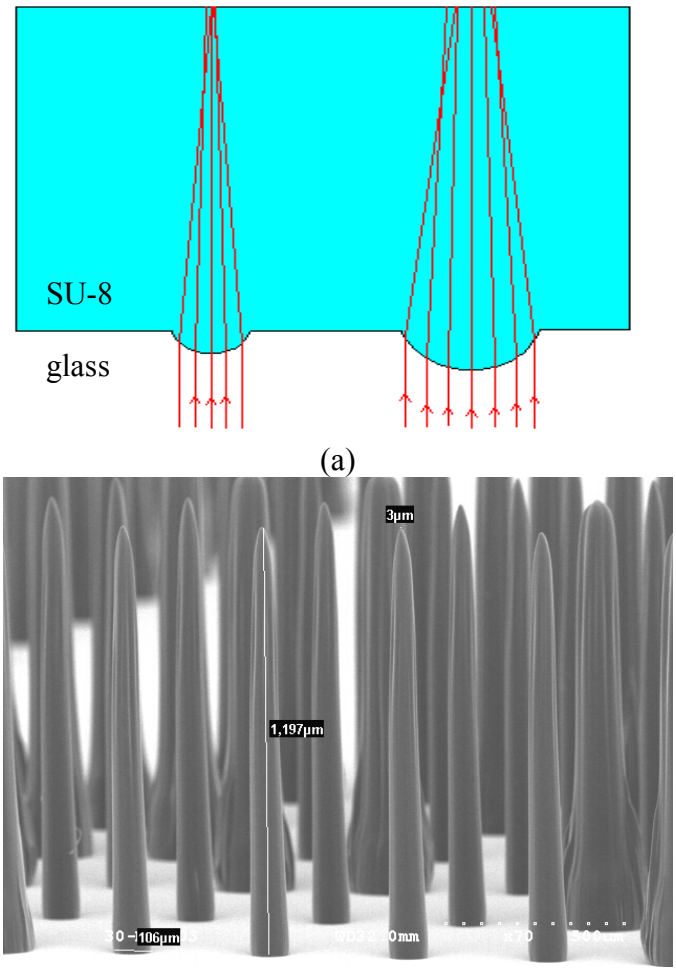
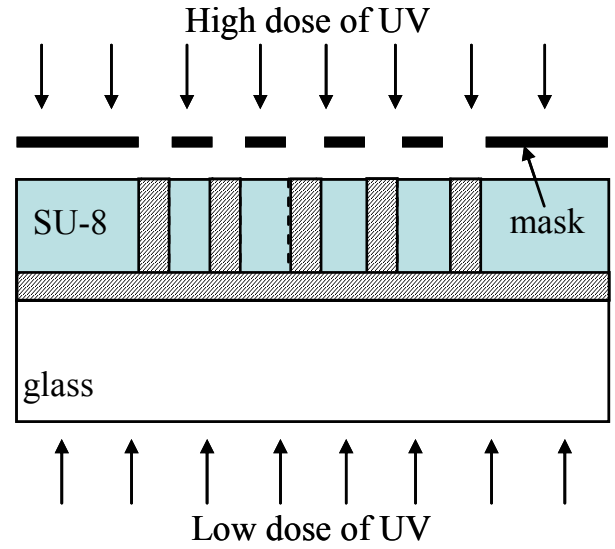
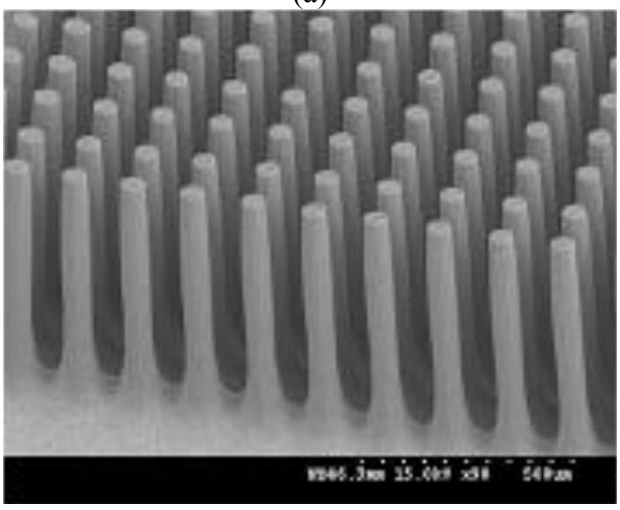



***Figure 3.19.*** *High-aspect-ratio tapered structure using integrated lens technique: (a) Ray trace simulation for the integrated lens; (b) Fabricated structure [74].*




(a)

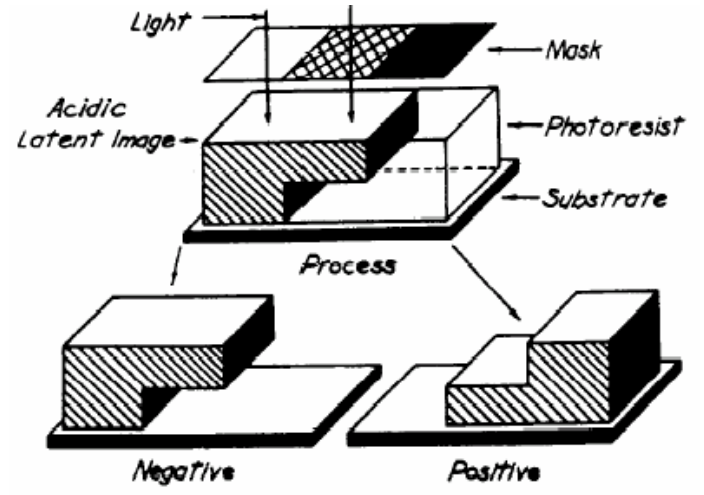


(b)

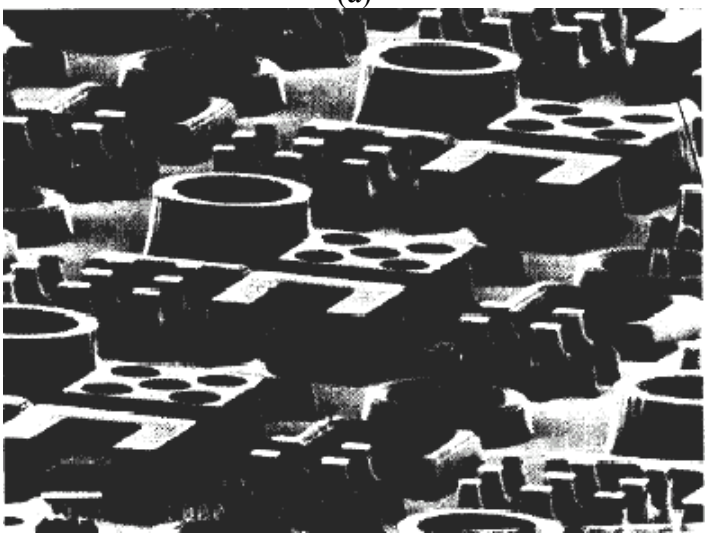
***Figure 3.20.*** *Unitary polymer substrate and column structures: (a) Schematic of the exposure scheme; (b) Fabricated structures [75].*

## 3.4. Multi-exposure Technique

Feely and co-workers at Rohm and Haas showed a 3-D thick photoresist process using their dual-tone photoresist [76, 77], where they demonstrated dual-tone resist chemistry combined with optical dose-controlled UV exposure could generate various patterns such as steps or overhangs as shown in Figure 3.21. Multi-step or continuous




(a)



(b)

***Figure 3.21.*** *Three dimensional patterning: (a) Latent image formation and processing using Rohm and Hass dual-tone resist; (b) Example of the types of features [77].*

structures can be achieved by single exposure and single development with a grey-tone mask [78]; however, often the required high resolution mask is too expensive for practical usage. Alternatively, multi-exposure processes with separate mask sets and controlled exposure time have been utilized for various applications, including RF inductors [79] and inkjet nozzles [80] both using a positive-tone phororesist and microchannels using a negative tone epoxy, SU-8 [81].

In this section, a double-exposure-single-development process used for high-aspect-ratio bridge fabrication is discussed. While the SU-8 multi-exposure-single-develop technique described in [81] utilized anti-reflection coatings in order to control the thickness of the upper portion of the device, the technique described here relies on the control of the baking steps after the second exposure and the UV source selection for the second exposure to achieve the final structure.

### 3.4.1. Fabrication

A fabrication process for a bridge or a channel structure using a double-exposure-single-development technique with SU-8 is detailed in Figure 3.22. SU-8 25 with a thickness of 1 mm is coated on a substrate. The thickness is controlled by weighing the proper amount of SU-8 on a substrate and placing it on a hot plate. The reduced viscosity of SU-8 at high temperature makes the SU-8 uniformly spread over the substrate on the well-leveled hot plate, resulting in self-planarization. The thick epoxy is then soft-baked for 72 hours on the hot plate at 95 °C (a). Full UV optical dose (i-line UV source; 365 nm, 9000 mJ/cm$^2$) is applied through a mask to create a latent image of the column or the

channel wall (b). A post-exposure bake is performed on the hot plate for 1 hour at 95 °C. Before it is developed, a shallow optical dose is applied to form the latent image of the top bridge or the channel cover layer (i-line UV source; 365 nm, 100 mJ / $cm^2$) (c). In order to get the top portion of SU-8 effectively crosslinked, the post-exposure bake is performed in an *oven* (20 min ~ 1 hour, 95 °C) instead of on a hotplate. The structure is

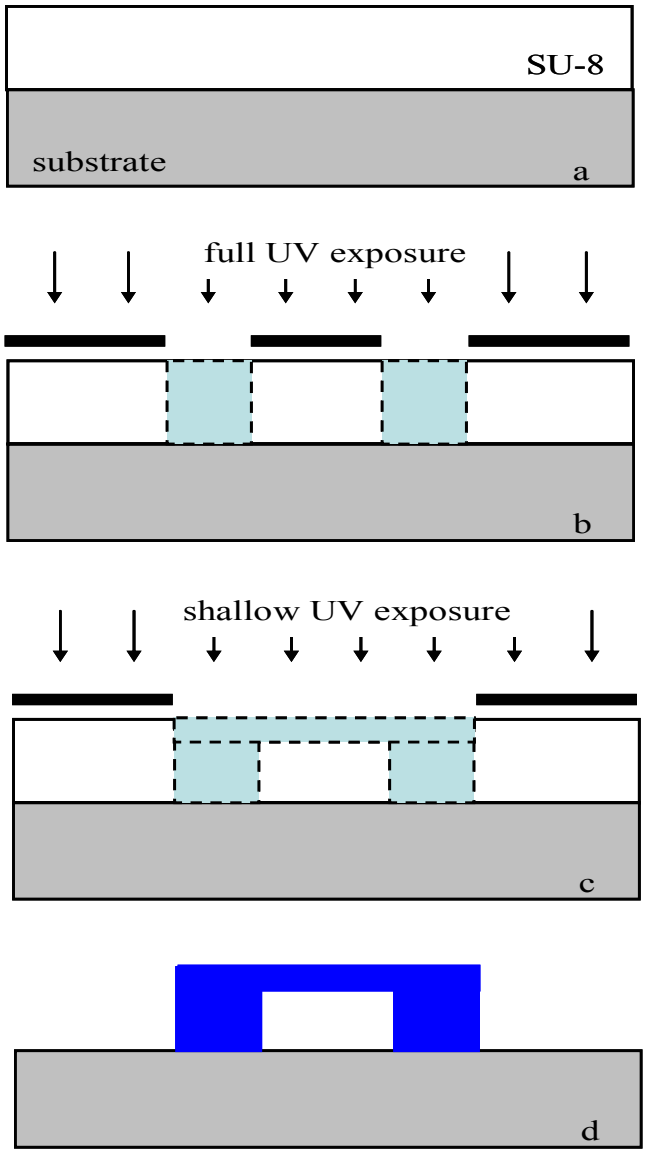



***Figure 3.22.*** *Fabrication process for a bridge or a channel structure using a double-exposure-single-development technique.*

developed in SU-8 developer, propylene glycol monomethyl ether acetate (PGMEA) for 3 hours to complete the process (d).

### 3.4.2. Characterization and Discussion

In the case of using a hotplate for the second post-bake instead of an oven, the heat energy from the bottom is not effectively transferred to the top portion through the thick polymer layer and polymerization of the top portion does not occur. Or if it does occur, the mechanical strength is very weak, the bridges are very loose, and they can move and stick to a neighboring bridge during development as shown in Figure 3.23.

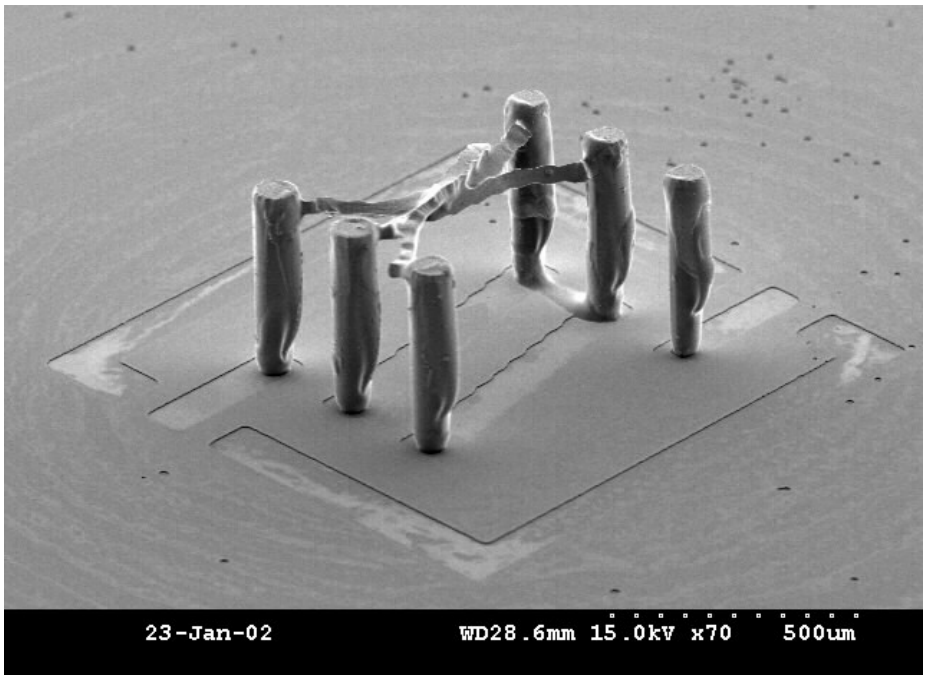
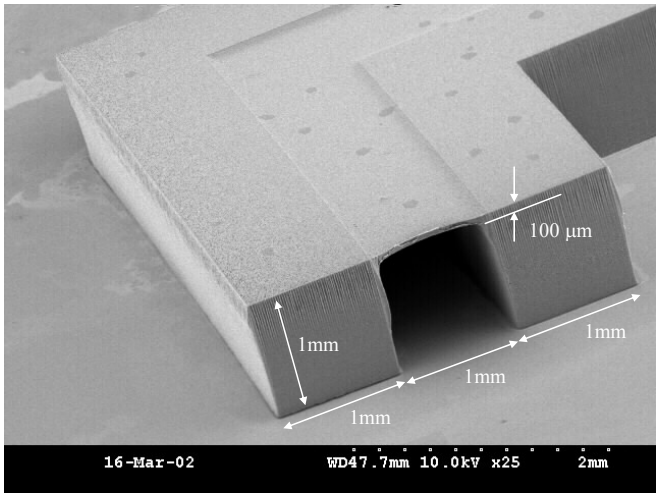
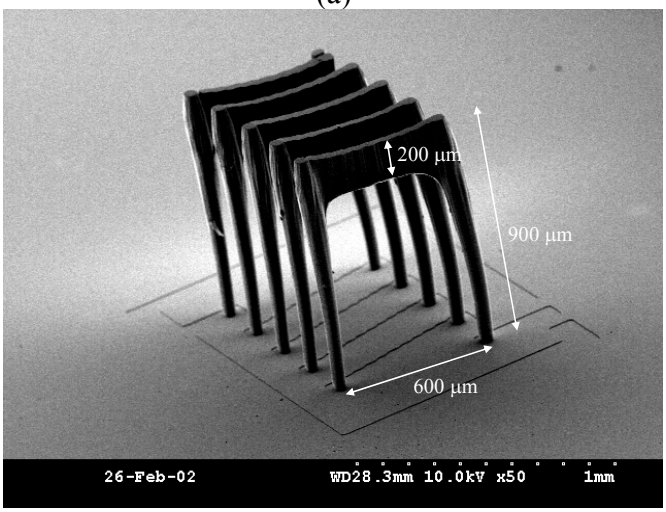



***Figure 3.23.*** *Distorted bridges during the development due to poorly polymerized top portion of SU-8 in the case of using a hotplate for the second post-exposure bake.*




(a)



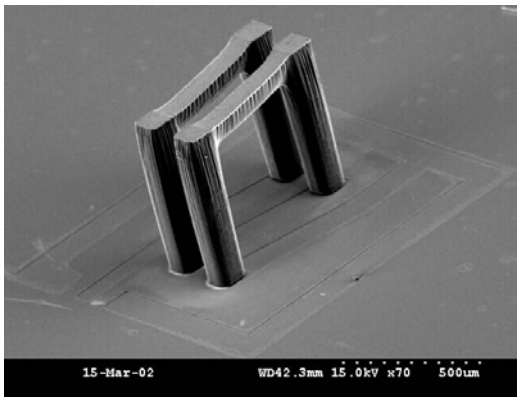

(b)

***Figure 3.24.*** *Successfully fabricated structures: (a) Microfluidic channel; (b) Bridges connecting two columns.*

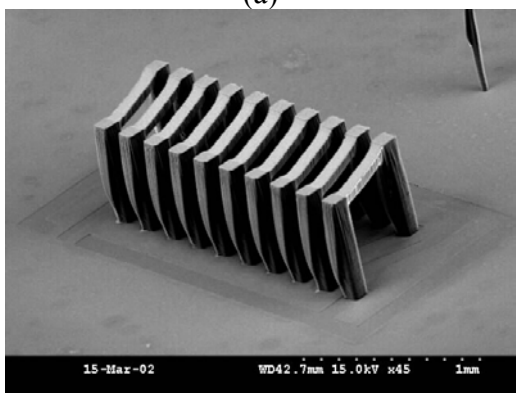
In the case of using an oven for the second post-bake, the thickness of the bridge is controlled by the optical dose and the post-exposure baking time. Figure 3.24a and 3.24b show a microfluidic channel and a bridge successfully fabricated using this process. The channel has a width of 1 mm, a height of 1 mm, and a cap thickness of 100 μm, which has been in the oven for 30 minutes while the bridge has a length of 600 μm, a height of 900 μm, and a bridge thickness of 200 μm, which has been in the oven for 40 minutes.

Various SU-8 structures for RF applications are shown in Figure 3.25: a solenoid-type inductor, a transformer, and a spiral-type inductor.

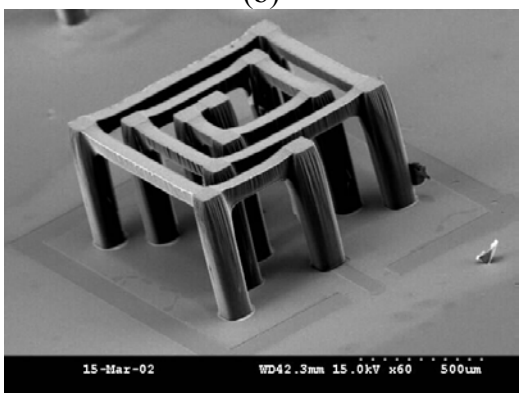
Alternatively, the bridge thickness could be controlled by using a different UV




(a)




(b)




(c)

***Figure 3.25.*** *SU-8 backbone structures for RF applications: (a) Solenoid-type inductor; (b) Transformer; (c) Spiral-type inductor.*

source. Microchem SU-8 is optimized for near-UV (350-400 nm) exposure. This formulation of SU-8 is less sensitive to light with wavelength above 400 nm, and high absorption of incident light with wavelength below 350 nm is observed. The UV absorbance of SU-8 as a function of wavelength is shown in Figure 3.26 [82]. Optical energy with a wavelength shorter than 350 nm is absorbed in the topmost portion and SU-8 below a certain depth becomes a UV-free region. Using a multiwavelength exposure approach, thickness control could be much more efficient than achievable with a single UV source.

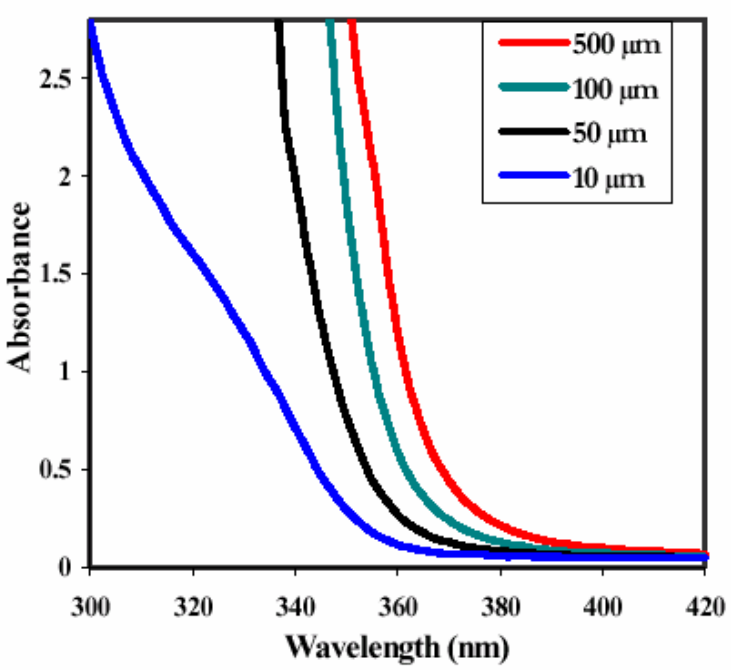



***Figure 3.26.*** *Energy absorbance of Microchem SU-8 as a function of wavelength of the UV source [82].*

## 3.5. Inclined Patterning

More complex 3-D structures can also be implemented by employing an inclined patterning scheme. Structures with inclined sidewalls realized by inclined synchrotron radiation exposure were reported [83 – 85]. However, this approach is quite expensive for general laboratory usage due to special radiation source and mask requirements. Meanwhile, an inclined mold for a rotor with tilted legs was achieved by UV exposure applied to a positive photoresist [86]. Recently, inclined exposure processes using SU-8, negative-tone photodefinable epoxy, and its applications have been reported [87 – 89].

In this section, SU-8 based inclined processes are discussed from two structural points of view: a vertical screen structure fabrication and an inclined structure combined with laser ablation technique.

### 3.5.1. Vertical Screen Filter Structure [88]

There are two approaches for the inclined exposure scheme. One is a conventional front-side inclined exposure, in which an SU-8 coated substrate in contact with an optical mask is tilted at a certain angle and is exposed. The other is to use reverse-side exposure through a UV-transparent substrate, in which the substrate has a pre-patterned opaque metal layer. SU-8 is coated on the substrate, and the substrate is turned over and exposed at the desired angle. Figure 3.27 details the fabrication process with reverse-side exposure. A chromium-coated glass plate is used as a substrate. After patterning of the chromium for channel and filter definition, SU-8 is coated on the plate to a thickness that will

ultimately define the channel height (a). After the SU-8 is baked, the substrate is turned over and multiply exposed at different angles of inclination from multiple directions in order to form latent images of the vertical meshes as well as the flow channel walls. This exposure is followed by a post-exposure bake to cross-link the SU-8 (b). Before developing, as discussed in the previous section, a low energy dose exposure through a second mask to link the ends of the filter screen is optionally utilized (c). A single develop step forms the filters as well as the channels simultaneously (d).

Since the refractive indices of SU-8, glass, and air are different, the incident light is

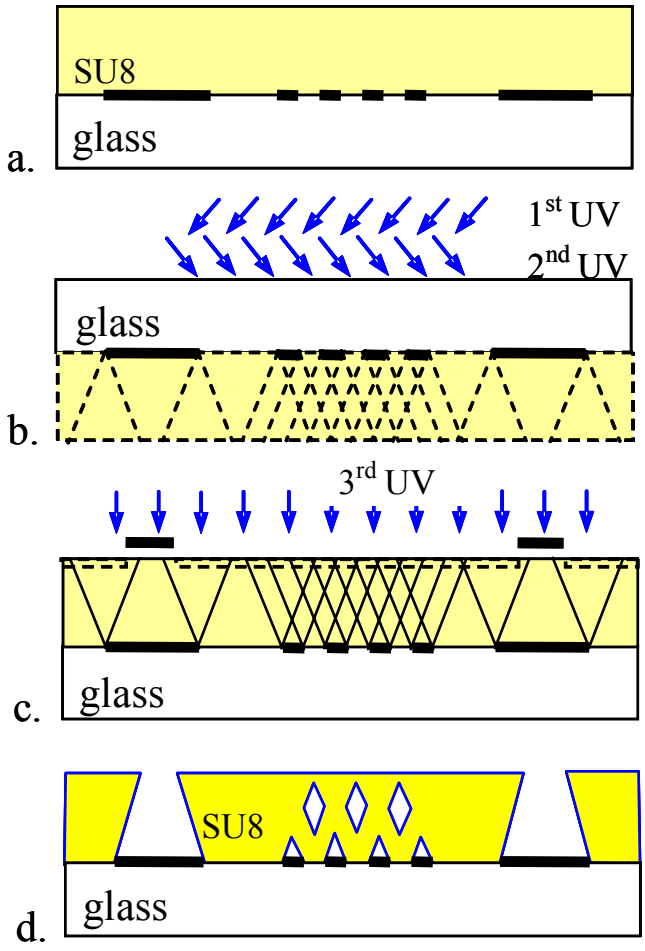



***Figure 3.27.*** *Fabrication process for vertical screen filter structure using multiple inclined exposures.*

refracted at each interface of two materials. The relationship between refractive indices and refractive angles is given by Snell's law for the three layer system in Figure 3.28.

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 = n_3 \sin\theta_3 \qquad (3.2)$$

where $n_1$, $n_2$, and $n_3$ are the refractive indices of air, glass, and SU-8, respectively, and $\theta_1$, $\theta_2$, and $\theta_3$ the incident angle in air, the refracted angle in glass, and the refracted angle in SU-8, respectively. The final refracted angle in SU-8 can be obtained if the refractive index of air $n_1$, the refractive index of SU-8 $n_3$, and the incident angle $\theta_1$ are known as in Equation 3.3.

$$\theta_3 = \sin^{-1}\frac{n_1}{n_3} \qquad (3.3)$$

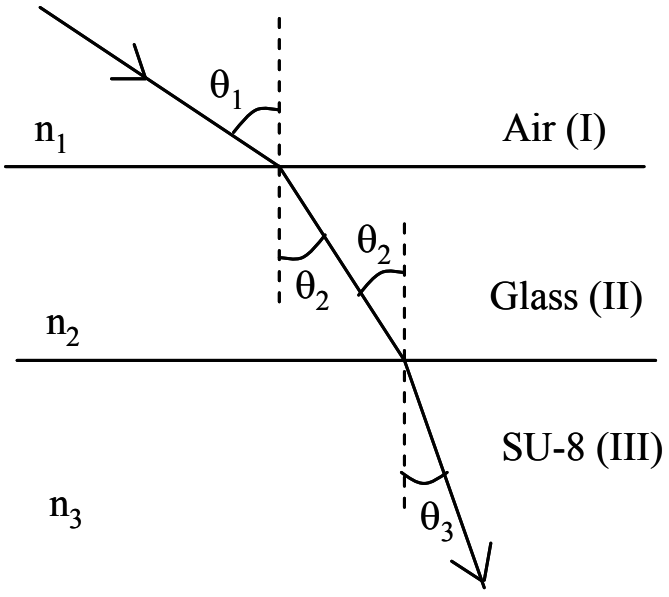
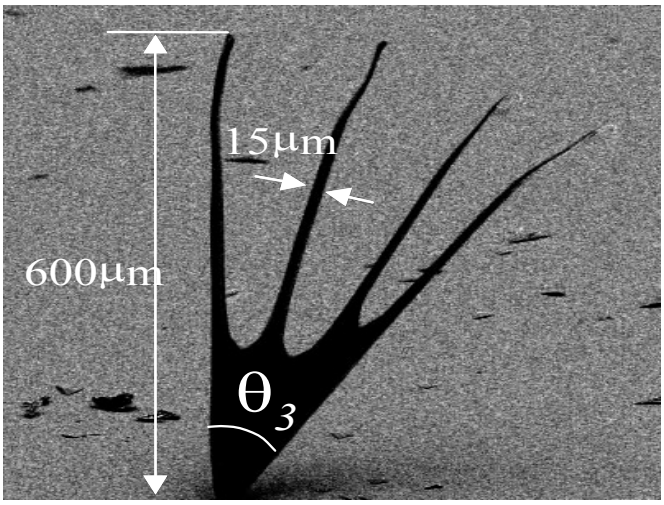
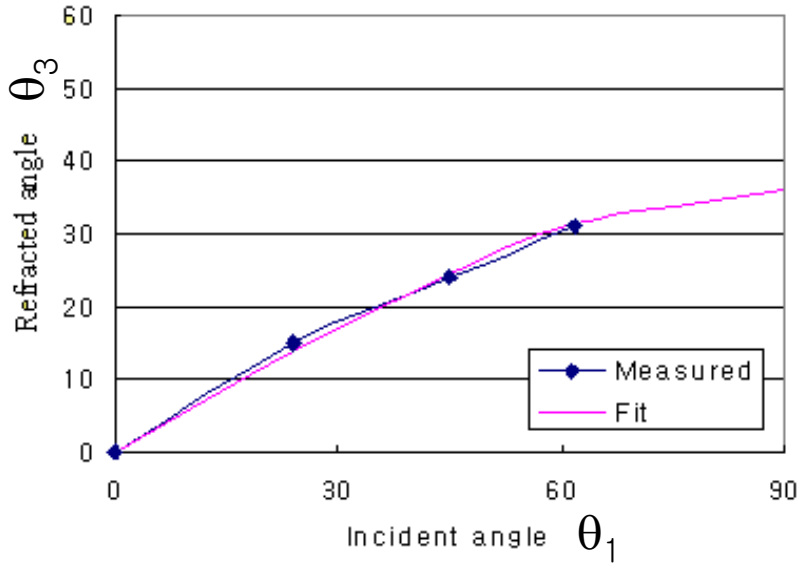



***Figure 3.28.*** *Light refracted at the interfaces due to different refractive indices of materials.*

Figure 3.29a shows a 600 μm thick SU-8 pattern exposed through a 15 μm diameter window with different angles of UV incidence using the reverse-side exposure technique (i-line UV used). The measured refracted angles are 0°, 15°, 24°, and 31° for incident angles of 0°, 24°, 45°, and 62°, respectively, in Figure 3.29b. Curve fitting using Snell's law ($n_1 \sin\theta_1 = n_3 \sin\theta_3$) gives a refractive index of about 1.7 for SU-8, which is in




(a)




(b)

***Figure 3.29.*** *Angular dependence of exposure: (a) SU-8 pattern multiply exposed with different incident angle; (b) Refracted angle vs. incident angle.*

agreement with the literature value [90].

Figure 3.30 shows a fabricated vertical screen filter structures [88]. A mask layout with 50 μm space and 50 μm width of transparent square array is depicted in Figure 3.30a, in which each array row is separated by 150 μm. An incident angle of 48° results in a refracted angle of approximately 26°, and the resultant diamond shape opening has a 50 μm horizontal diagonal and a 100 μm vertical diagonal. While the bottom channel width is 1100 μm, the upper channel width becomes narrower (720 μm) resulting from reverse-side exposure, with a channel height of 390 μm in Figure 3.30b.

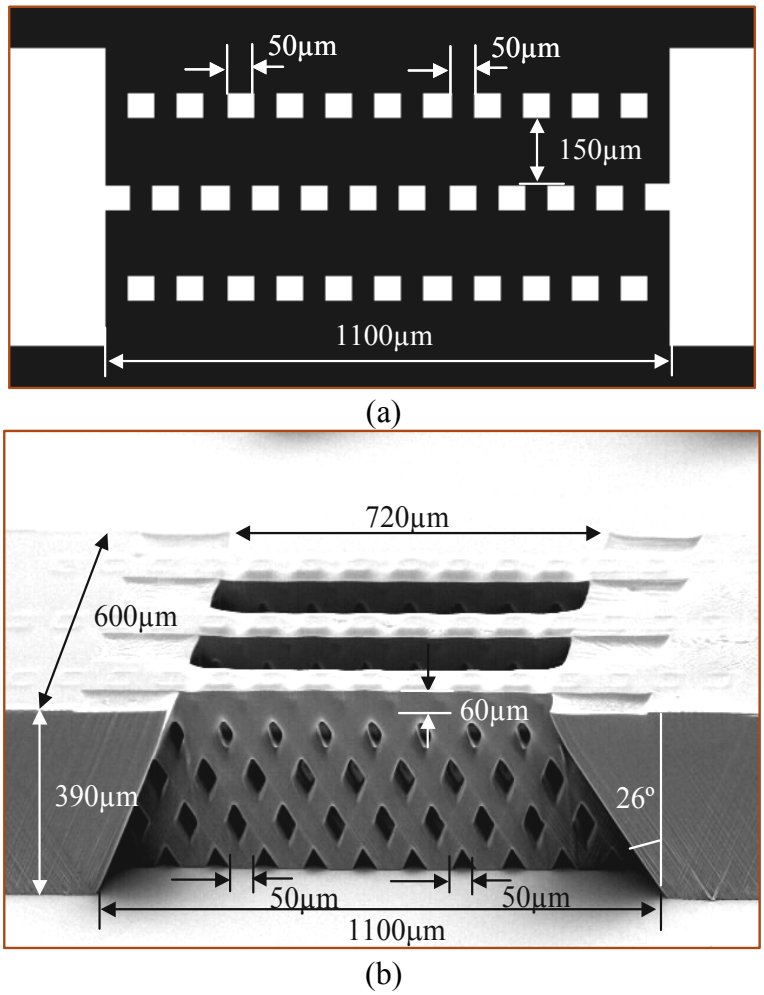



***Figure 3.30.*** *A vertical screen filter: (a) Mask layout; (b) Resultant vertical screen filter.*

The achievable mesh size is related to the mesh dimension in the mask and the screen height (another viewpoint of aspect ratio: horizontal mesh width to total screen height). Aspect ratio of 20:1 seems to be the limit of the uniform mesh with SU-8 under current baking and developing conditions. Figures 3.31a and 3.31b show the fabricated different sized meshes of 80 μm and 2 μm, respectively, where the heights are 500 μm and 40 μm, respectively.

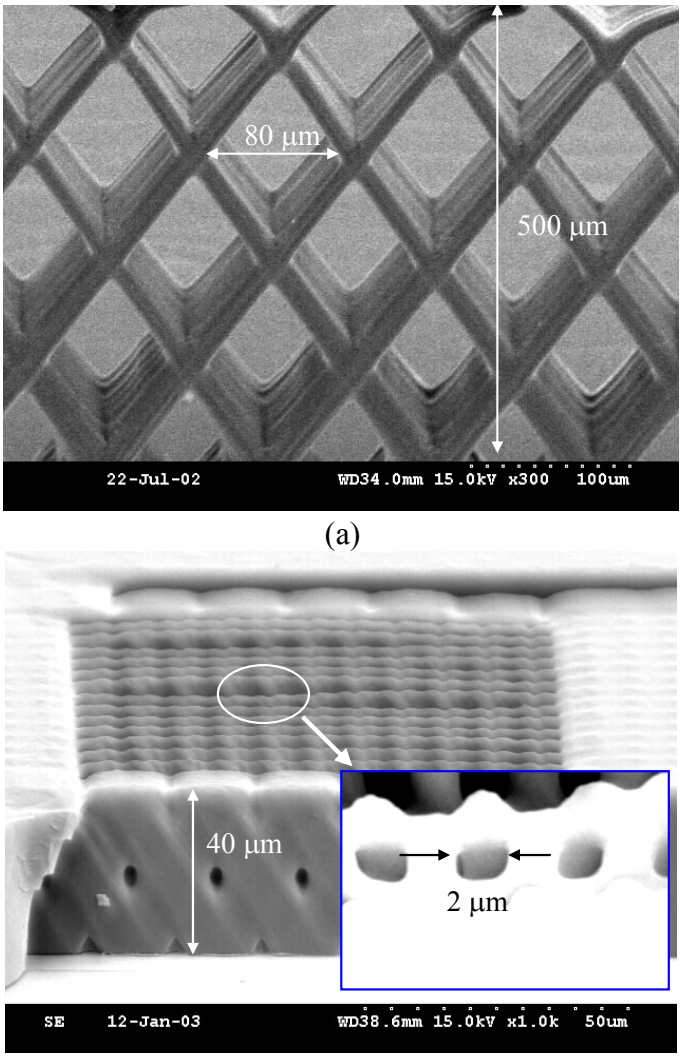



***Figure 3.31.*** *Different sized meshes: (a) Large mesh with horizontal diagonal of 80 μm; (b) Small mesh with horizontal diagonal of 2 μm.*

In Figure 3.32, three different mesh-sized vertical screen filter structures are simultaneously fabricated using two inclined exposures, one shallow vertical exposure, and a single development with a single mask. Each vertical screen filter has a different mesh size. The resultant horizontal diagonal extent of the threads of each screen mesh is 57.3 μm, 27.3 μm, and 10.0 μm, respectively in Figure 3.33. Uniform opening distribution is observed.

Figure 3.34 shows a periodic vertical screen filter placed within a long channel [88]. The vertical screen filter structures with appropriate metallization can be used for millimeter wave or terahertz applications such as waveguides, resonance devices, or photonic band gap (PBG) structures.

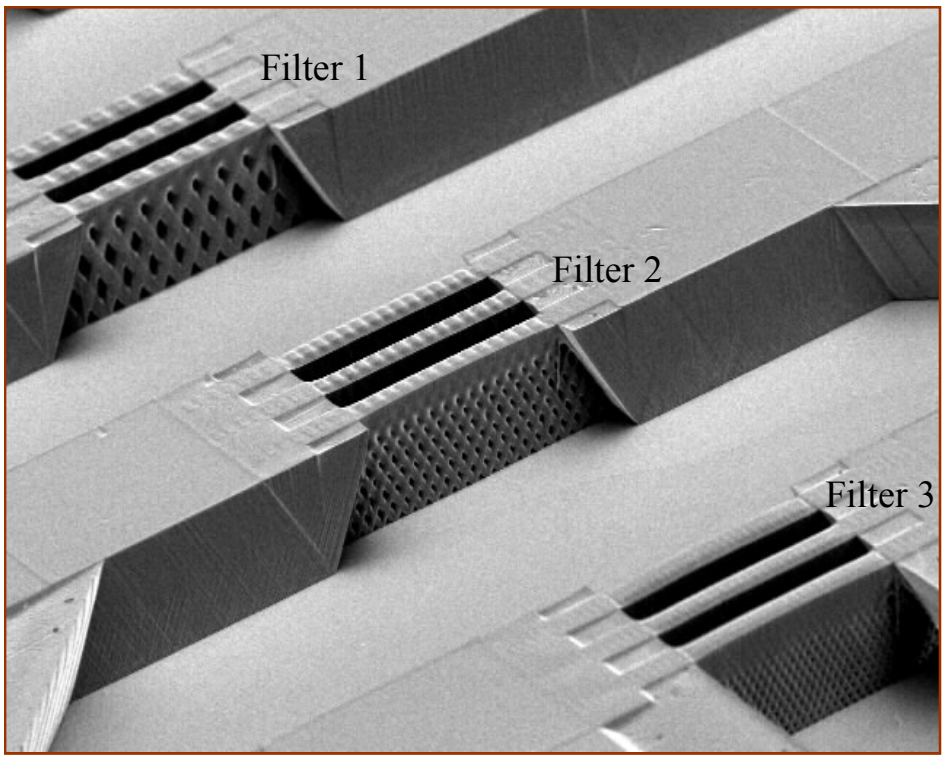
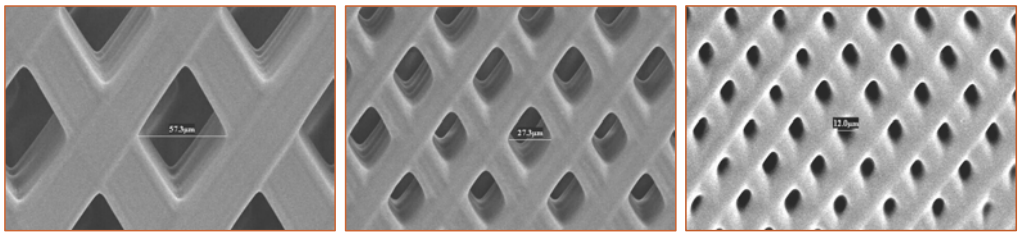
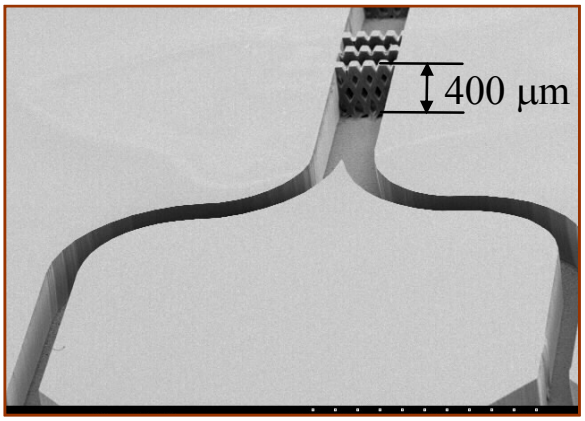



***Figure 3.32.*** *Simultaneously fabricated three integrated filters and channels with different mesh sizes.*

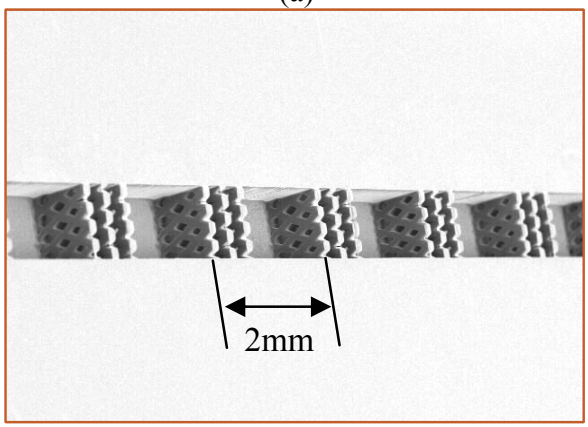


(a) (b) (c)

***Figure 3.33.*** *Different mesh sizes of the integrated filter structures: (a) Filter 1; (b) Filter 2; (c) Filter 3. Horizontal diagonal has been measured to be 57.3 μm, 27.3 μm, and 10.0 μm, respectively.*




(a)




(b)

***Figure 3.34.*** *Microfluidic channel with periodically loaded screen filters: (a) Connection of two fluidic channel; (b) Channel with periodic screen filters.*

### 3.5.2. Inclined Structure with Laser Ablation [91]

The inclined exposure technique combined with laser ablation technique is introduced. An appropriately-spaced tube array or parallel channel array is formed with an intentional angle of inclination, followed by masked excimer laser ablation at normal incidence. This approach allows variation of microfluidic ports up and down the third dimension with a single masked ablation exposure.

Figure 3.35 details the fabrication process. A chromium-coated glass plate is used as a substrate. After patterning of the chromium for channel definition, SU-8 photosensitive

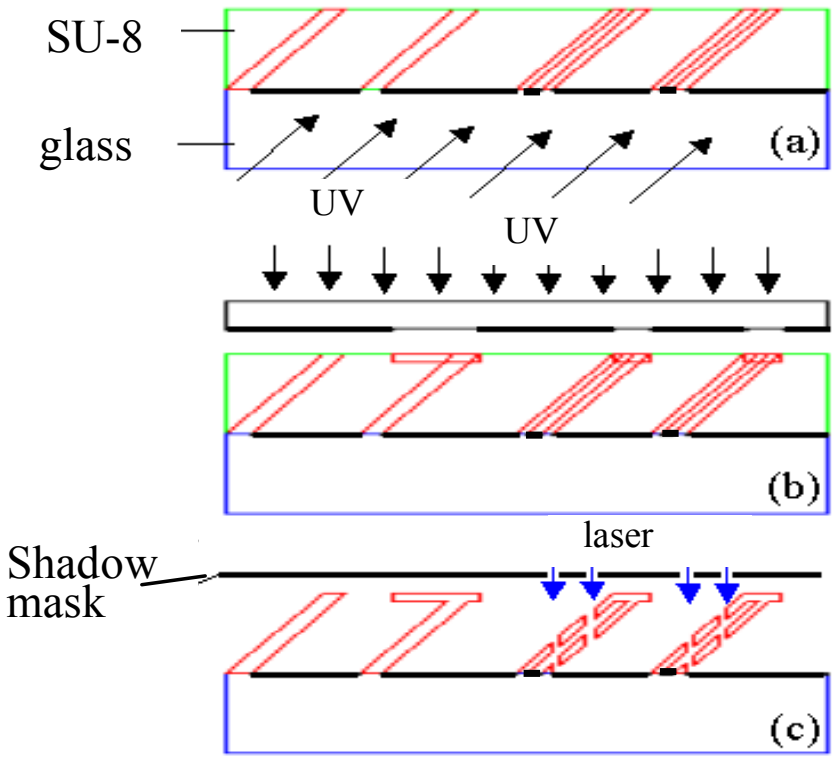
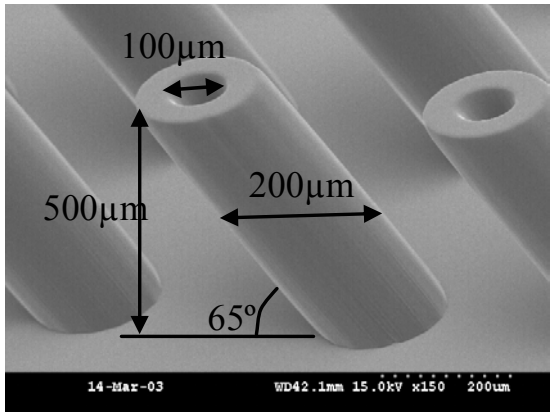
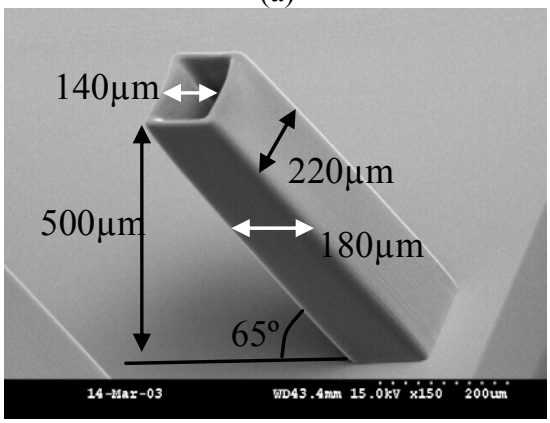



***Figure 3.35.*** *Fabrication process of inclined structures combined with laser ablation technique.*

epoxy is coated on the plate to a thickness that will ultimately define the channel height. After the SU-8 is baked, the substrate is turned over and exposed at an angle of inclination in order to form latent images of the inclined channel walls through the thickness of the epoxy. This exposure is followed by a post-exposure bake on a hot plate to cross-link the SU-8 (a). Before developing, a low energy dose exposure is applied through a second mask to form the caps of the channels (double exposure technique of Section 3.4 is applied). The multiply exposed structure is then post baked in an oven (b). A single develop step forms the inclined branch channels as well as the wide channels. Finally, excimer laser ablation (λ=193 nm) through a metal shadow mask forms the




(a)




(b)

***Figure 3.36.*** *Fabricated SU-8 hollow columns: (a) Circular hollow column array; (b) Rectangular column.*

vertically-distributed microfluidic ports (c).

Figure 3.36 shows fabricated hollow columns; (a) a circular column array, (b) a rectangular column array. Both are 500 μm tall and are inclined at an angle of 25º from the vertical.

Figure 3.37 shows a laser drilled inclined hollow column 500 μm in height with three laser-drilled holes on the sidewall. The laser beam spot size was 25 μm, the horizontal spacing between the holes was 50 μm, and the vertical spacing (resulting from the interaction of the horizontal spacing with the angle of inclination) was approximately

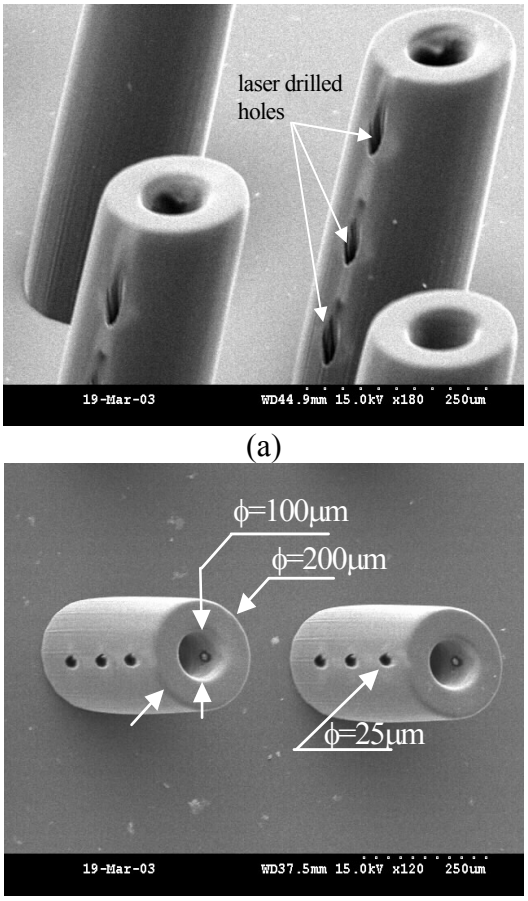
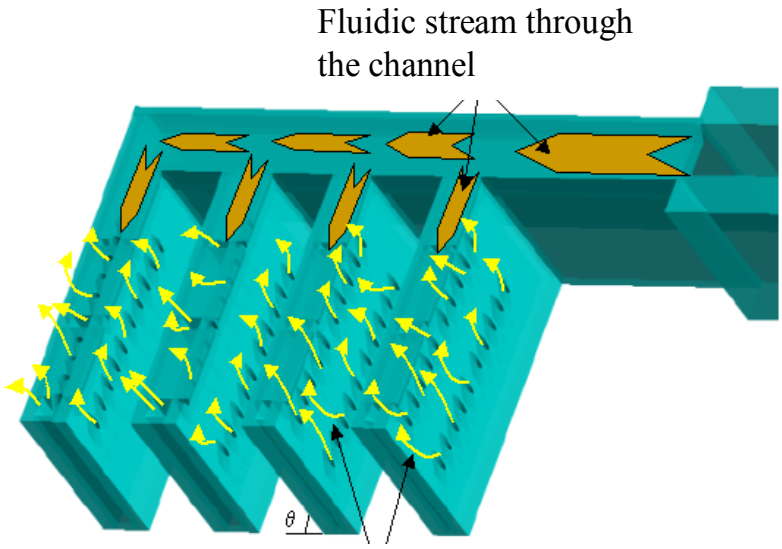


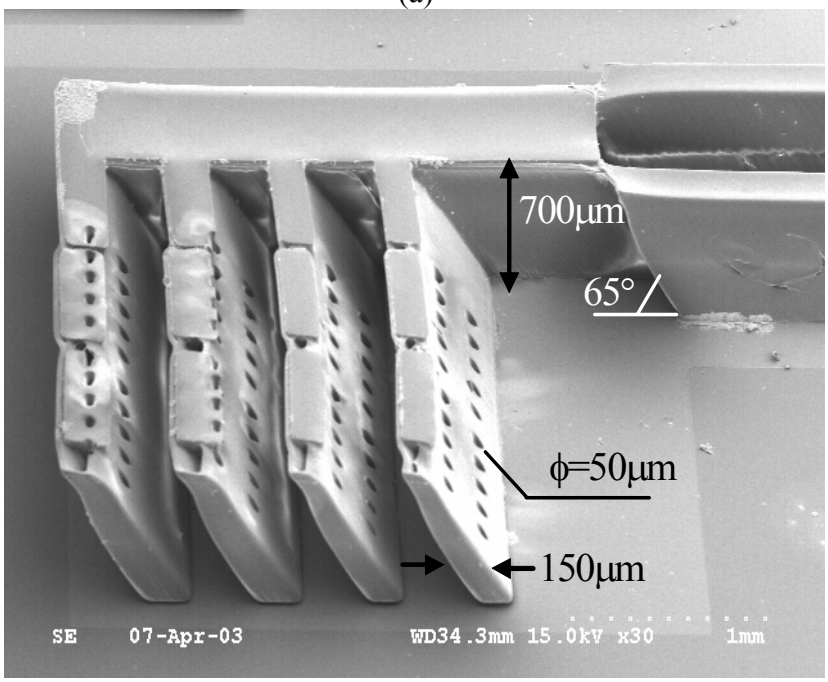

***Figure 3.37.*** *Fabricated SU-8 hollow columns with laser drilled holes: (a) Oblique view; (b) Top view.*

100 μm.

Figure 3.38 shows a schematic view of the inclined channel array and an SEM of the fabricated device. The array has four inclined channel branches, each bearing laser-drilled holes. The height of the channel is 700 μm; the wall thickness of the channel is 50 μm; and the widths of the branch channels are 50 μm for the narrow channel and 100 μm for the wide channel, respectively. The angle of inclination is approximately 25° from the vertical axis. The laser-ablated holes have diameters of 50 μm and an array pitch of 150 μm. The fluid is supplied through the entrance of the wide channel and the fluid branches to the four smaller inclined channels. The left two branches have larger channel widths to take into account the pressure drop through the long fluidic microchannels.




(a)




(b)

***Figure 3.38.*** *Four inclined channel branches with laser drilled holes: (a) Schematics; (b) Fabricated structure.*

# CHAPTER IV

# DEVELOPMENT OF ARCHITECTURES FOR RF COMPONENTS

This chapter describes two RF device architectures: a reduced intermodulation distortion (IMD) ferroelectric tunable capacitor and a compact tunable LC module.

## 4.1. Architecture for Reduced Intermodulation Distortion (IMD) in Ferroelectric RF Tunable Capacitors

Among various ferroelectric materials, barium strontium titanate, $Ba_{1-x}Sr_xTiO_3$ (BST), is a very attractive RF tunable material due to its large field-dependent permittivity, high dielectric constant, large breakdown voltage, and relatively low loss tangent. With BST as a dielectric layer of an RF capacitor, we can take advantage of the device size reduction from its high dielectric constant and a simple implementation of a tuning device with its electric-field-dependent permittivity. In order to have high tunability in RF capacitors, a narrow gap is desirable, which in turn results in a self-

modulation effect when the input RF signals are in the order of the DC bias voltage level. In fact, this *intermodulation distortion (IMD)* is one of the fundamental issues restricting the usage of tunable capacitors for linear devices such as phase shifters or tunable filters.

In a voltage tunable capacitor, the IMD is directly proportional to the tunability of the capacitor, as expressed in Equation 4.1 [92]:

$$IMD \propto V_{RF}/V_{DC} \qquad (4.1)$$

where $V_{RF}$ is the amplitude of the RF signal voltage and $V_{DC}$ is the voltage required for tuning. One approach to improve IMD performance in high RF-power handling devices is to make the DC tuning voltage much higher than that of any RF voltage level. While this approach is effective, tuning voltages required to achieve acceptably low levels of IMD often exceed 100V. Therefore, this approach to reduced IMD is severely limited by the desire to keep tuning voltages relatively low. Although no significant current is drawn to bias the capacitor, a system problem results in supplying the high static potentials required for this approach.

This section describes a device architecture that addresses the reduced IMD issue by means of a capacitor that has an additional, highly resistive DC bias structure constructed within the RF gap capacitor [93, 94]. This additional structure allows decoupling of the RF signal and DC tuning voltage levels, thereby enabling low IMD structures at low tuning voltages. The first subsection will describe a device concept. It is followed by two subsections: (1) design architecture I, where discussion is focused on the architecture for

the proof of concept, and (2) design architecture II, where discussion is focused on an architecture for further IMD improvement.

### 4.1.1. Concept

Two architectures are shown in Figure 4.1: (a) a gap capacitor with attached-bias-electrodes (ABE), having DC bias electrodes connected to the RF pads; and (b) a gap capacitor with isolated-DC bias-electrodes (IBE), which can be energized independently of the RF electrodes. Figure 4.1c shows the cross-sectional view of both geometries. The RF capacitor is a conventional microwave gap capacitor that uses thick and high conductivity electrodes to ensure high quality factor ($Q$-factor). In contrast, the DC bias structure is fabricated with high resistivity interdigital structures. At low frequencies, such as those used to change the tuning bias voltage, the high resistivity lines present negligible impedance compared with that of the gap capacitor and the full tuning voltage appears across the lines, changing the permittivity of the structure and therefore the capacitance. However, at signal frequencies (i.e. RF frequency), the impedance of the bias lines exceeds that of the gap capacitor itself, so the RF current travels through the (permittivity-tuned) ferroelectric material. Because the RF field is effectively isolated by the high resistance of the bias structure, no degradation in IMD performance occurs. Furthermore, if the resistivity is kept high enough, no noticeable degradation in capacitor $Q$ will occur at the operating frequency, since the RF field will preferentially interact with the low-loss, low-impedance BST capacitor.

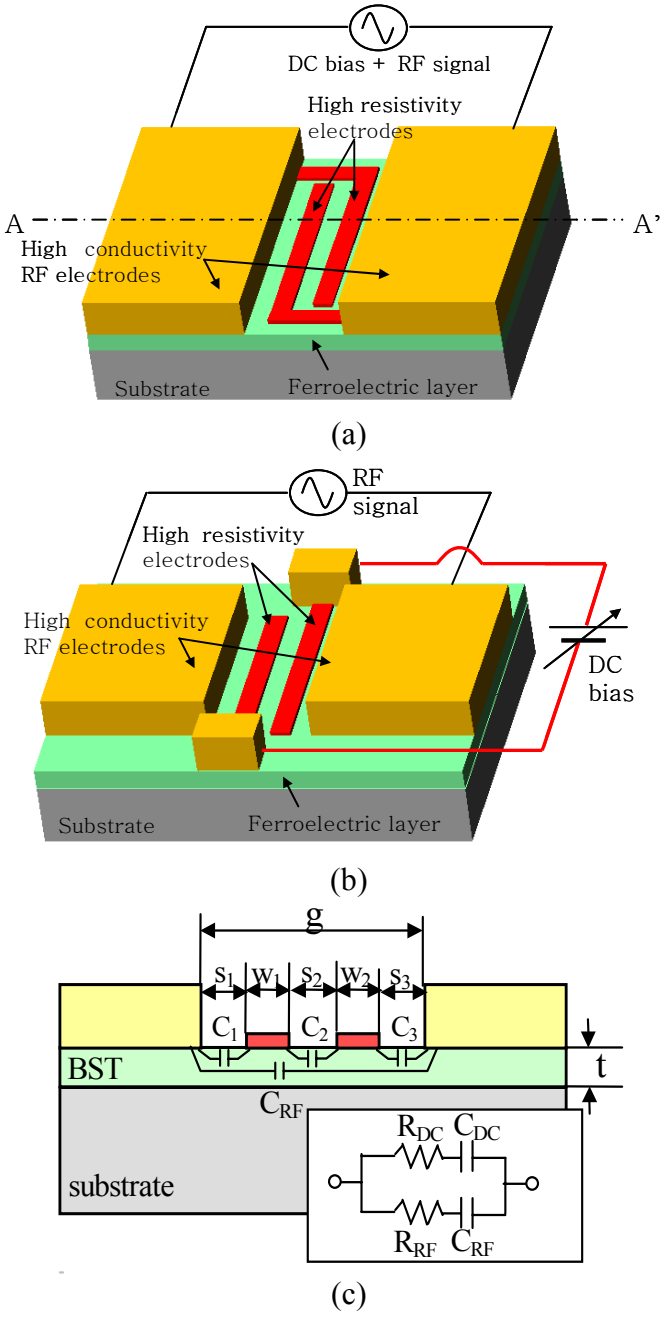



***Figure 4.1.*** *Two architectures of a reduced IMD ferroelectric gap capacitor: (a) Attached-bias-electrode (ABE) pattern; (b) Isolated-bias-electrode (IBE) pattern; (c) Cross-sectional view of A-A' (an equivalent circuit is shown in the inset).*

### 4.1.2. Design Architecture I

Figure 4.2 shows two conventional gap capacitors, one with a wide gap and the other with a narrow gap. While the narrow gap capacitor requires less area and lower DC voltage for required capacitance and tunability compared with the wide gap geometry, it will have degraded IMD performance, as expected from Equation 4.1. For applications such as phase shifters and tunable filters, the IMD performance must be maintained. Hence, wide gap capacitors are mainly used at the cost of both device real estate and high required tuning voltage.

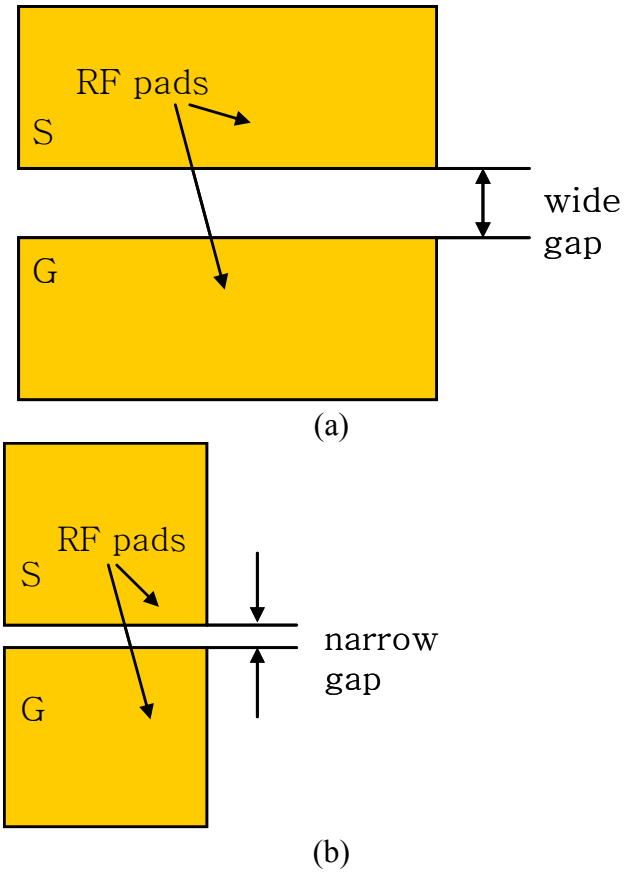



***Figure 4.2.*** *Conventional gap capacitors (top view): (a) Wide gap capacitor (type I); (b) Narrow gap capacitor (type II).*

In contrast to the conventional gap capacitor, consider a gap capacitor with highly resistive bias electrodes in the RF gap. Figure 4.3 shows three DC electrode design schemes for this type of capacitor. Figure 4.3a shows a gap capacitor with short bias electrodes placed inside the RF gap parallel to the RF field and attached to the RF electrodes (the so-called short attached-bias-electrode or short ABE structure). Note that the DC electric field generated between the short bias electrodes is perpendicular to that of the RF field. Figure 3b shows a gap capacitor with long bias electrodes placed inside the RF gap perpendicular to the RF field and attached to the RF electrodes (the so-called long attached-bias-electrode or long ABE structure). Note that the DC electric field generated between the long bias electrodes is parallel to that of the RF field. Finally, Figure 4.3c shows a capacitor with long bias electrodes but those electrodes are electrically isolated from the RF pads (the so-called long isolated-bias-electrode or long IBE structure). Similarly to the long ABE structure, the DC electric field of the long IBE structure is also parallel to that of the RF field. The overall gap capacitor architectures are summarized in Table 4-1.

Now that each geometry has been described, the electrical performance will be analyzed. Consider the cross-sectional view of the long ABE capacitor (type IV) and its associated equivalent circuit as shown in Figure 4.1c. In the circuit, the upper branch consists of an equivalent series resistance of the highly resistive conductor line $R_{DC}$ and a capacitance $C_{DC}$ from the combined effects of $C_1$, $C_2$, and $C_3$. The lower branch has a series resistance of pads $R_{RF}$, and an RF capacitance $C_{RF}$ with gap $g$ defined primarily by the high-permittivity ferroelectric layer between the highly conductive conductors. It is assumed that the capacitance through the ferroelectric layer is dominant due to the

relatively high dielectric constant of the ferroelectric material, and the capacitance through the substrate and the air may be ignored. Therefore, $C_{RF}$, and the associated $Q$ as determined by $R_{RF}$, is determined by the geometry of the metal. It is clear that for reduced IMD operation, the cutoff frequency of the DC bias structure should be well below the

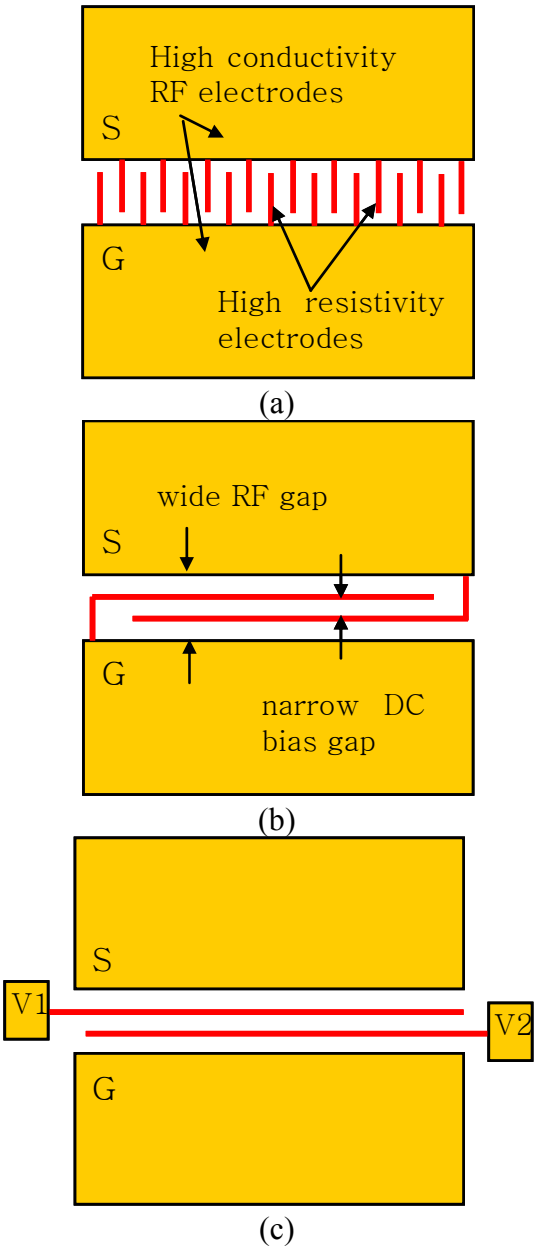



***Figure 4.3.*** *Gap capacitors with high-resistivity bias electrodes inside the gap (top view): (a) Short attached-bias-electrode (ABE) capacitor (type III); (b) Long attached-bias-electrode (ABE) capacitor (type IV); (c) Long isolated-bias-electrode (IBE) capacitor (type V).*

RF frequency of operation of the tunable capacitor. This implies that $R_{DC}$ should be as high as possible. The only restriction is that the time constant formed by this structure, $\tau_{DC} = R_{DC}\, C_{DC}$, may limit the rate at which adjustment of the capacitance, i.e. tuning, may occur. At signal frequencies, the impedance of the RF path is much lower than that of the DC path, and therefore the RF current travels through the ferroelectric material; however, the permittivity of this ferroelectric material has been adjusted by low frequency tuning voltage applied by means of the DC path. In this way, the tuning and capacitance functionalities of the device are decoupled, and reduced IMD can be achieved at low tuning voltage.

**Table 4-1.** Summary of gap capacitor architectures

| | | Abbreviation | Features |
|---|---|---|---|
| **conventional gap capacitor** | **type I (Fig. 4.2a)** | **wide gap capacitor** | **- wide gap<br>- large area<br>- high tuning voltage<br>- low IMD** |
| | **type II (Fig. 4.2b)** | **narrow gap capacitor** | **- narrow gap<br>- small area<br>- low tuning voltage<br>- large IMD** |
| **gap capacitor with high resistivity electrodes inside RF gap** | **type III (Fig. 4.3a)** | **short attached-bias-electrode capacitor (short ABE capacitor)** | **- wide RF gap (→ low IMD)<br>- narrow DC bias gap<br>- DC field perpendicular to RF field<br>- DC electrodes attached to the RF electrodes<br>- low tuning in RF range** |
| | **type IV (Fig. 4.3b)** | **long attached-bias-electrode capacitor (long ABE capacitor)** | **- wide RF gap (→ low IMD)<br>- narrow DC bias gap<br>- DC field parallel to RF field<br>- DC electrodes attached to the RF electrodes<br>- large tuning in RF range** |
| | **type V (Fig. 4.3c)** | **long isolated-bias- electrode capacitor (long IBE capacitor)** | **- wide RF gap (→ low IMD)<br>- narrow DC bias gap<br>- DC field parallel to RF field<br>- DC electrodes isolated from the RF electrodes<br>- large tuning in RF range<br>- flexibility of biasing scheme** |

### 4.1.3. Design Architecture II

A wide gap capacitor has multi-pairs of high resistivity electrodes within the RF gap area in Figure 4.4, where $G$ is RF gap and $g$ is dc bias gap. When both dc bias and RF signal ($v(t)=V_0+V_1\sin\omega t$) are applied to the electrodes, since the resistivity of dc bias electrodes is designed to be high enough to prevent RF signal from traveling through it, only dc bias $V_0$ reaches the high resistivity electrodes and forms the electric field $E_{dc}$ between narrow gap $g$. Fringing field changes the permittivity of the underlying ferroelectric layer. The dielectric constant of the ferroelectric layer ($\varepsilon_{r\_BST}$~1000) dominates compared to those of substrate ($\varepsilon_{r\_sapphire}$~10) and air ($\varepsilon_{r\_air}$~1); therefore, most of the RF signal travels through the permittivity-tuned ferroelectric layer.

In the case that $V_0$ and $V_1$ are at a similar voltage level, the electric field due to $V_1$ ($E_{RF}=V_1/G$) is small compared to that of the dc bias ($E_{dc}=V_0/g$), and therefore the self-modulating effect is reduced due to the gap ratio. As the number of pairs of dc electrodes in the gap increases, the difference between $G$ and $g$ also increases. This increase results in the lowering of the self-modulation effect due to the RF signal at a given DC tunability.

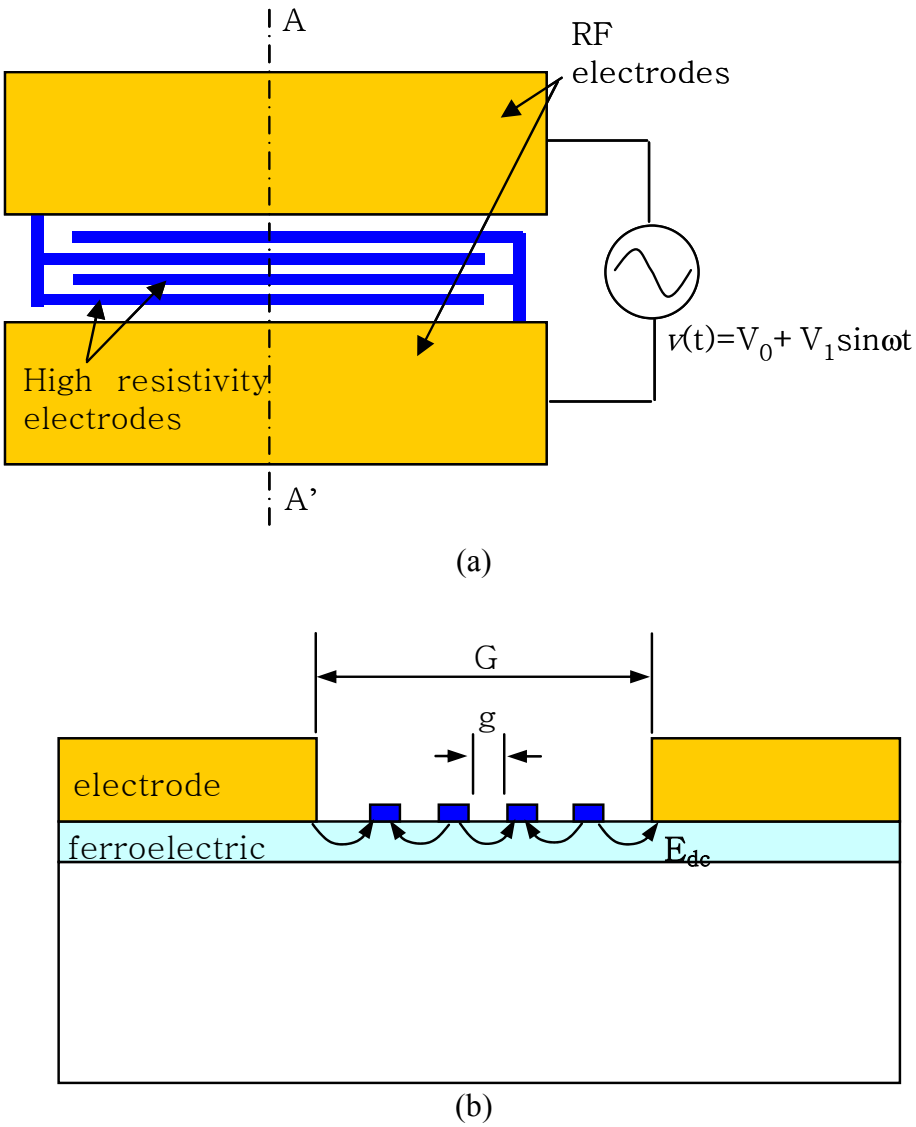


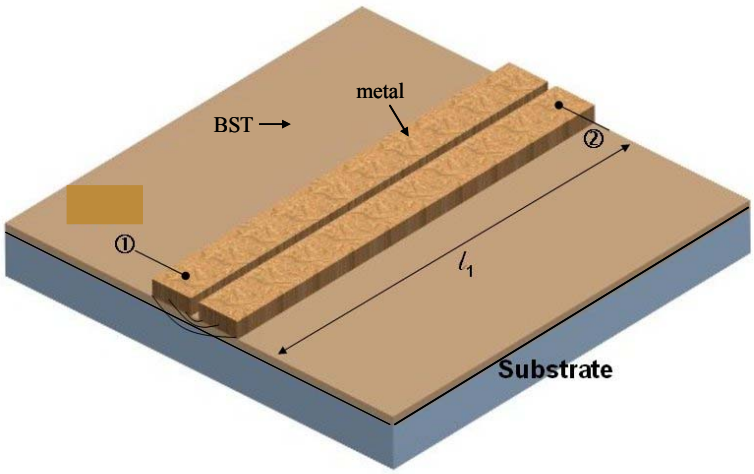

***Figure 4.4.*** *Reduced IMD capacitor with multiple pairs of high resistivity electrodes within an RF gap: (a) Top view (type IV); (b) Cross-sectional view of A-A'.*

## 4.2. Compact Tunable LC Module

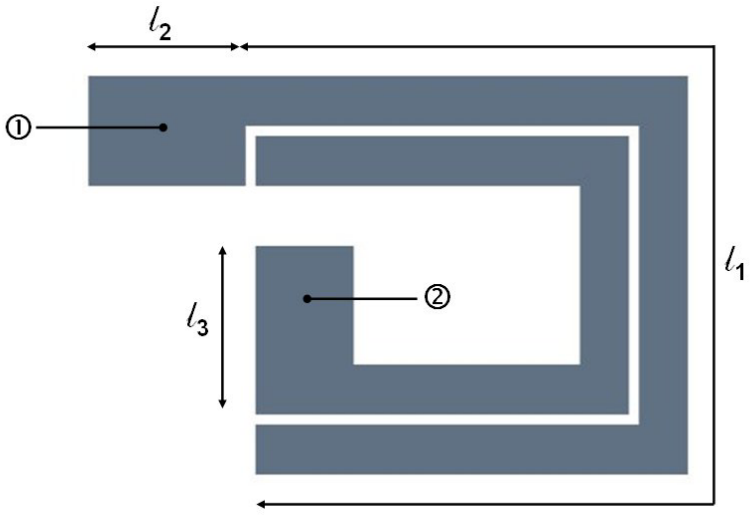
It has been previously observed that most chip or board space is occupied by passive components in RF systems [95]. Some RF devices such as phase shifters, LC filters, or matching circuits are often implemented with inductors and capacitors only [36, 96, 97]. Instead of designing and fabricating inductors and capacitors separately, it would be useful if LC modules are built in the form of a compactly coupled building block, thereby the device footprint can be reduced and the parasitics between the inductors and the capacitors can be taken into account as a part of the module at the design stage. The LC modules can be tuned by combining them with dielectric materials having electric-field-dependent permittivity or magnetic-field-dependent permeability. In this section, an architecture of a tunable compact LC module is introduced using a distributed gap capacitor formed in an inductively coupled shape on ferroelectric barium strontium titanate (BST), which has electric field dependent permittivity.

A long distributed gap capacitor is formed on top of a ferroelectric substrate such as barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$: BST) in Figure 4.5a. Since the permittivity of BST changes with an electric field, the capacitance varies by applying dc bias between port1 and port2. When an inductive component is necessary in addition to the capacitor, it can be implemented by modifying its geometry as in Figure 4.5b, where capacitance is maintained as shown in Figure 4.5a by keeping the coupling length $l_1$, while inductance is increased by winding it in a spiral shape. The inductance can also be adjusted by varying the lengths $l_2$ and $l_3$. The final structure will be as small as a single inductor while the tuning functionality and capacitance are maintained.

The geometry of Figure 4.5b is simplified as in Figure 4.6a, which is a series connection of an inductive line and a variable capacitor. Then the inductive line is translated to a series connection of resistance and inductance in Figure 4.6b. Since all the components are in series, it is simplified to a $R_{eq}L_{eq}C$ resonance circuit, where $R_{eq}$ is an




(a)




(b)

***Figure 4.5.*** *Schematic of concept: (a) Straight gap capacitor; (b) Inductively wound gap capacitor.*

equivalent series resistance, $L_{eq}$ an equivalent inductance, and C a capacitance in Figure 4.6c. A compact tunable LC module based on this architecture will be fabricated in Chapter 5.3.

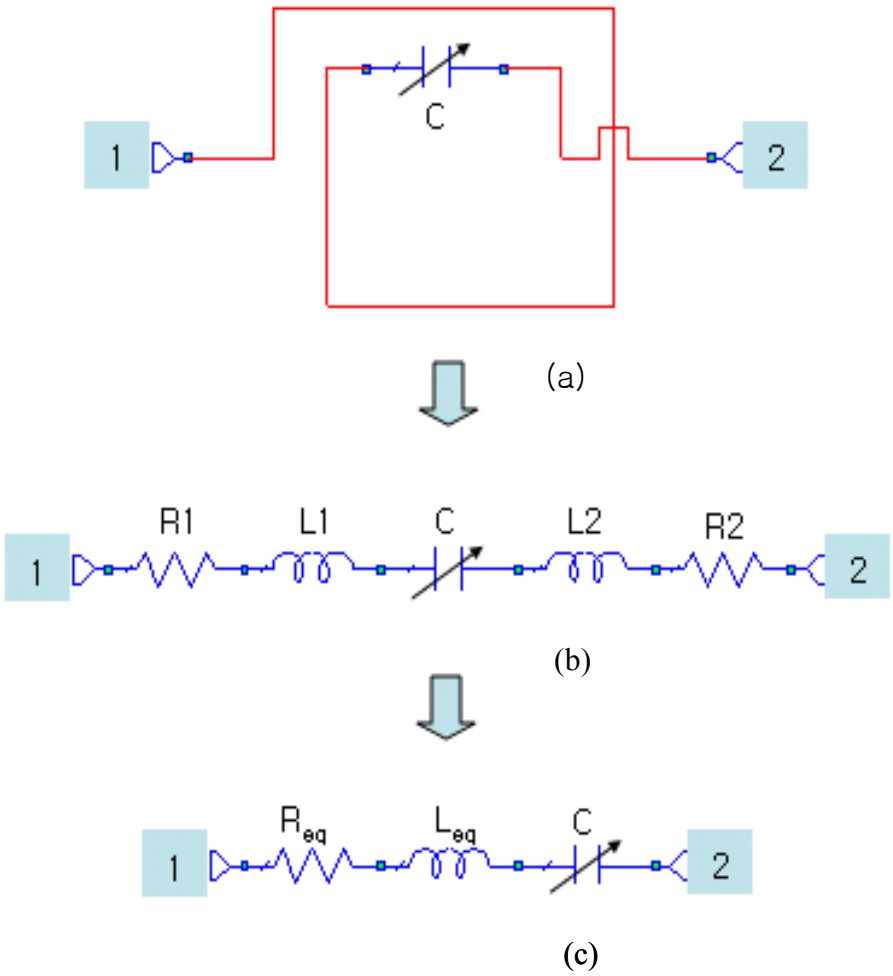



***Figure 4.6.*** *Equivalent circuit diagram: (a) Inductively wound gap capacitor; (b) Intermediate equivalent circuit; (c) Simplified RLC circuit.*

# CHAPTER V

# APPLICATIONS

Based on the previously introduced fabrication techniques and architectures, several RF components have been designed, fabricated, and tested. The structures include two solenoid type inductors: an embedded inductor and a high-aspect-ratio inductor based on epoxy-core conductors; two ferroelectric capacitors: a BST based gap capacitor with low-loss conductor and a reduced IMD gap capacitor; a BST based tunable LC module; and a W-band monopole antenna.

## 5.1. RF Inductors

Among many requirements for integrated RF inductors, an important issue is to minimize the parasitic effects, e.g., coupling capacitance between the inductors and the substrate, and loss caused by induced eddy currents in the substrate. A solenoid-type inductor is considered as a good candidate for an integrated type inductor due to low loss and low parasitics [22, 23]. In this section, two solenoid type RF inductors are introduced.

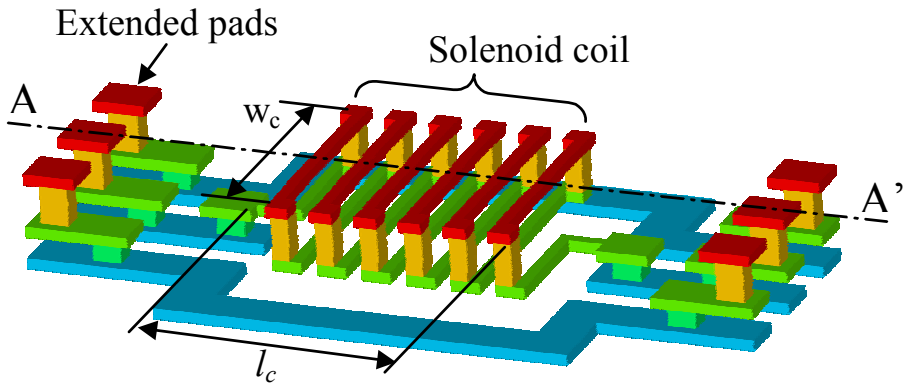
### 5.1.1. Embedded Inductors

Most previously reported micromachined RF inductors have the metallic coil parts overhanging in the air after substrate etching or sacrificial mold removal to minimize substrate effects. A drawback of these approaches is that the resultant etched wafer and/or inductor structures may be too delicate to withstand subsequent conventional injection-molding-based or other chip packaging approaches.

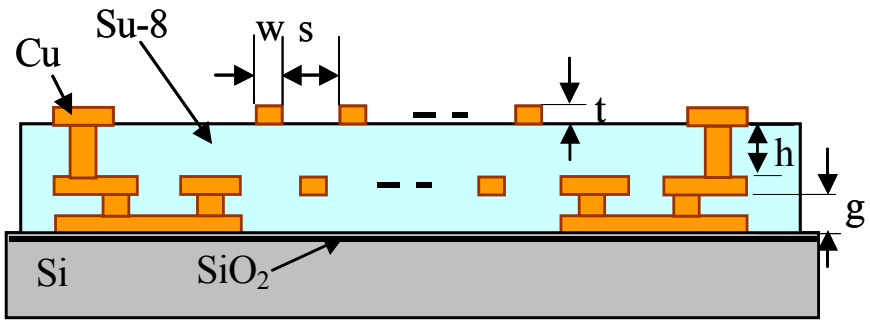
Here, surface micromachined, epoxy-embedded, high-Q electroplated inductors have been fabricated using the technique of *embedded conductors in polymer* introduced in Chapter 3. These inductors combine the desirable features of: (1) being supported by both electroplated posts and a deposited thick dielectric layer, thereby separating them from the lossy silicon substrate; and (2) being embedded in the epoxy molds from which they are formed, minimizing microphonics and allowing sufficient mechanical stability such that the chips bearing the inductors can be packaged using standard injection-molding processes. An additional processing benefit from the embedded structure is that the epoxy mold used to form the inductors need not be removed in a lengthy etch step. To demonstrate the compatibility of the reduced-parasitic, embedded inductor process with CMOS circuitry, four inductors are post-processed onto a foundry-fabricated RF CMOS power amplifier.

#### 5.1.1.1. Design and Fabrication

The schematic of an embedded solenoid inductor is shown in Figure 5.1, where the embedding mold layer is omitted in Figure 5.1a for the purpose of structural clarity and is presented in Figure 5.1b. A variety of inductor geometries have been designed and analyzed using an inductance calculation program, MEMCAD [98]. The main considerations for the design are: (1) to reduce coupling effects between the silicon (Si)




(a)




(b)

***Figure 5.1.*** *Schematic of solenoid inductor: (a) Perspective view (SU-8 mold is not illustrated for structural clarity); (b) Cross-sectional view of A-A'.*

substrate and the coil by separating them by a substrate gap $g$ and (2) to reduce turn-to-turn stray capacitance between the lines by orienting the lines in parallel [22] and by adjusting the spacing between lines $s$ and the layer-to-layer core height $h$. In the final design, a line spacing $s$, a core height $h$, and a gap $g$ of 60 μm, 40 μm, and 25 μm, respectively, have been used. The thickness $t$ of the metal layers is 10 μm and the line width $w$ of the coil is 20 μm. Since the skin depths of copper at 1 GHz and 10 GHz are approximately 2 μm and 0.66 μm, respectively, the designed $w$ and $t$ are not a limiting factor for high-Q inductors. In addition, inductors with varying numbers of turns and varying solenoid core width $w_c$ have been analyzed. To enable electrical probing of the test inductors, extended pads are designed since the inductor structure itself will be inaccessibly embedded in epoxy.

The inductor fabrication process is based on negative tone photosensitive epoxy (SU-8, Microchem, Inc.), negative photoresist (NR9-8000, Futurrex, Inc.), and copper (Cu) electroplating. The fabrication processes for test inductors and for inductors fabricated on CMOS circuitry differ slightly. For the test inductors, the first layer is copper and is patterned to form grounds in a ground-signal-ground (G-S-G) configuration as well as to form the extended pad connection. For the CMOS integrated inductors, the first layer is made of chromium/gold (Cr/Au) and is in contact with a CMOS aluminum (Al) pad. The rest of the process is the same for both inductors. The fabrication process for the inductor on CMOS is described in Figure 5.2.

Referring to Figure 5.2a, a Cr/Au pad layer (200 Å / 3000 Å) is deposited and patterned on the CMOS chip using a standard lift-off process. This layer serves as a contact layer between the CMOS circuitry and the inductors, and also protects the CMOS

probe pads from the acidic Cu electroplating bath. An SU-8 epoxy layer (25 μm) is spin-coated and patterned for the first via definition (Figure 5.2b). After seed layers (Ti/Cu/Ti) are deposited using a DC-sputterer, a thick (10 μm) negative photoresist NR9-8000 is spin coated and patterned for the lower metal layer and the first via hole (Figure 5.2c). Two metal layers (the first via hole and the coil lower metal layer) are formed simultaneously with a single electroplating step. After the first electroplating, the

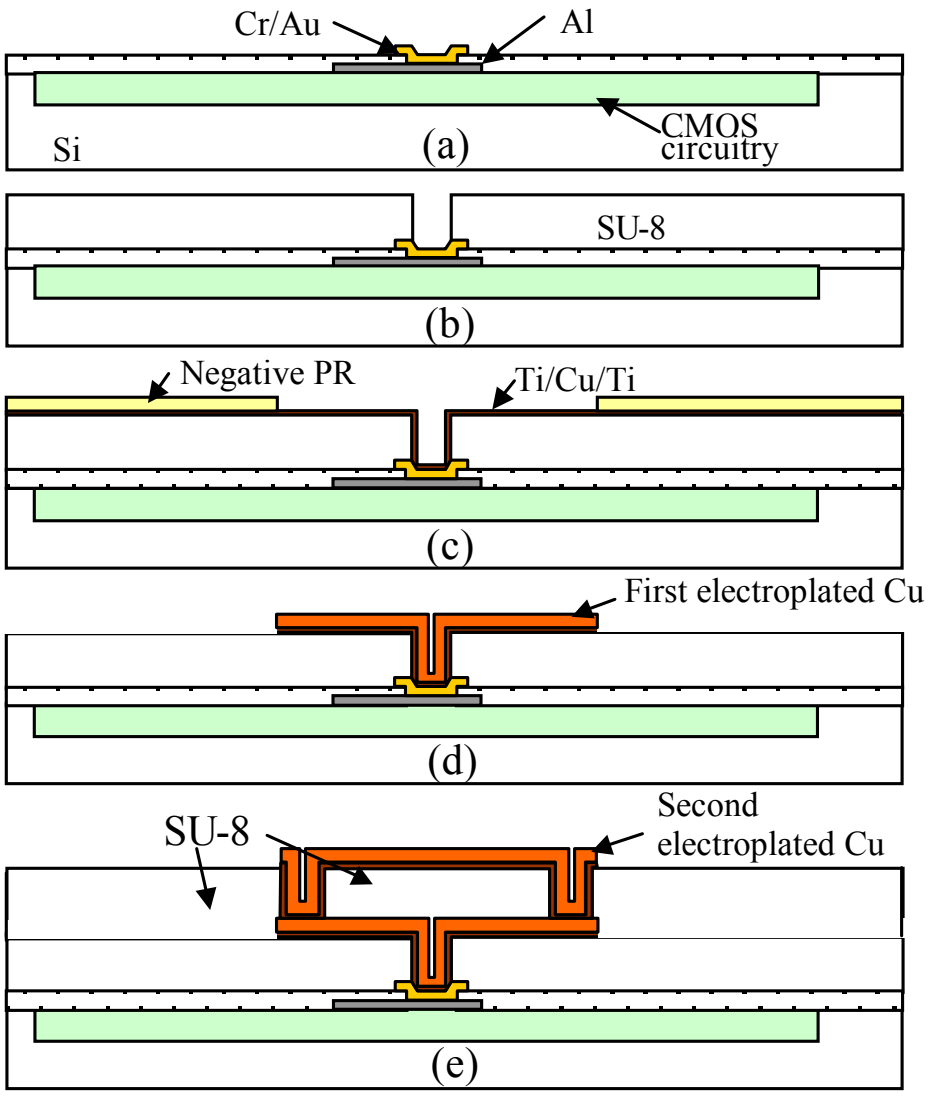


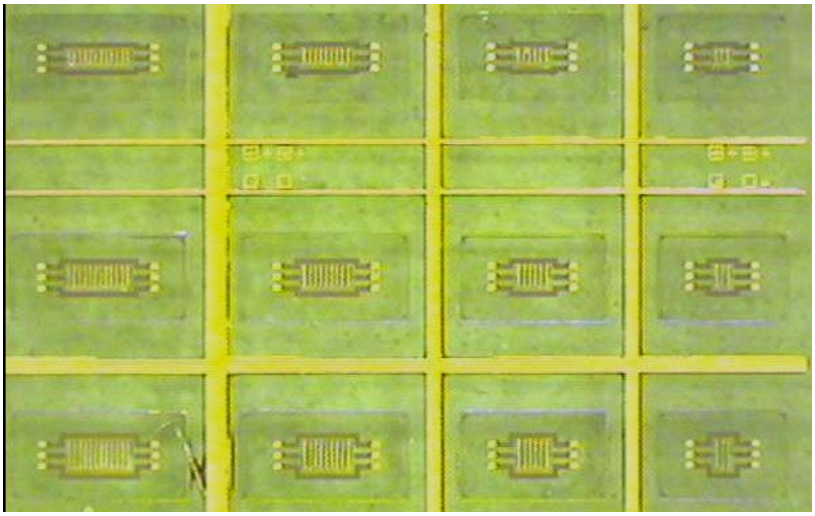

***Figure 5.2.*** *Fabrication process for the inductor on CMOS.*

photoresist mold and seed layers are removed, but the SU-8 mold surrounding the via as well as the electroplated Cu structure remains. Note that both the via post and the SU-8 mold mechanically support the entire solenoid coil thereafter (Figure 5.2d). Steps *(b)* through *(d)* are repeated for the next via (40 μm thick) and the coil upper metal layer. Note that the core of the embedded inductor is filled with SU-8 (Figure 5.2e). Since the core of the inductor has already been filled, and is mechanically robust, the inductance and Q-factor of the inductor are not expected to change after a subsequent packaging process, such as plastic injection molding. However, the electrical properties of the epoxy may influence the inductor properties in this configuration.

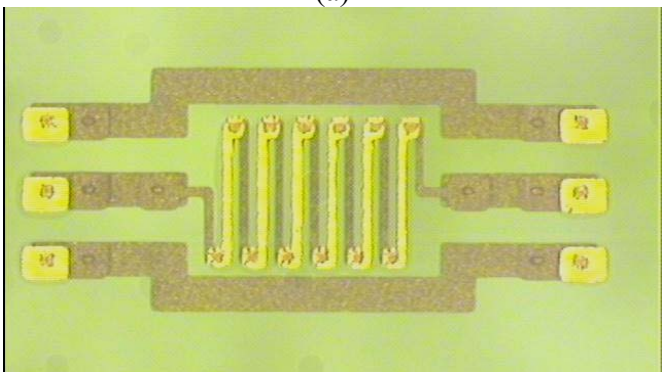
Figure 5.3 shows photomicrographs of fabricated test inductors. An inductor 'library' consisting of deices with various number of coil turns (3, 6, 9, and 12) and various core width (100 μm, 200 μm, 300 μm, and 400 μm) is shown in Figure 5.3a. (Note that the inductors with 400 μm core width are not captured in this figure due to a limited camera span). A top view and an oblique view of a 6 turn inductor with core width of 300 μm are shown in Figure 5.3b and 5.3c, respectively. Since epoxy is transparent, the embedded metal part as well as the exposed metal part can be seen. The brighter and the darker metal parts in Figure 5.3b are exposed metal and embedded metal portions, respectively.

Figures 5.4a and 5.4b show SEM views of a fabricated 6 turn embedded inductor. In Figure 5.4a, the exposed metal probe pads and upper metal of the coil can be seen while the embedded part cannot because the electron beam does not penetrate through the SU-8 epoxy to give an image. Note that the SEM image has been taken without applying a thin metal coating over the structure in this case and the nonuniform charge distribution

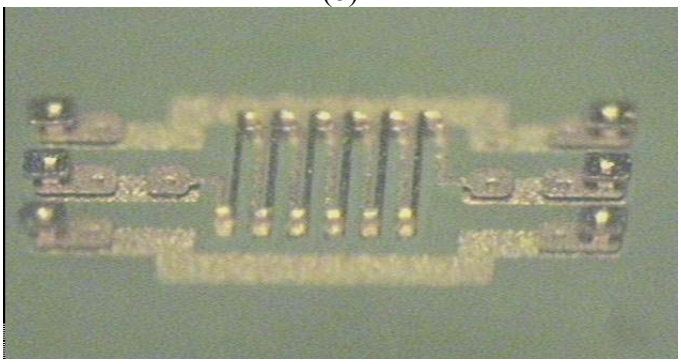
results in a discoloration on the SU-8 surface. Figure 5.4b shows an SEM view of the device after the embedding epoxy has been etched away for clarity. The solenoid coil is 25 μm above the Si substrate. The coil width *w* is 20 μm, the turn-to-turn pitch *p (= w+*



(a)



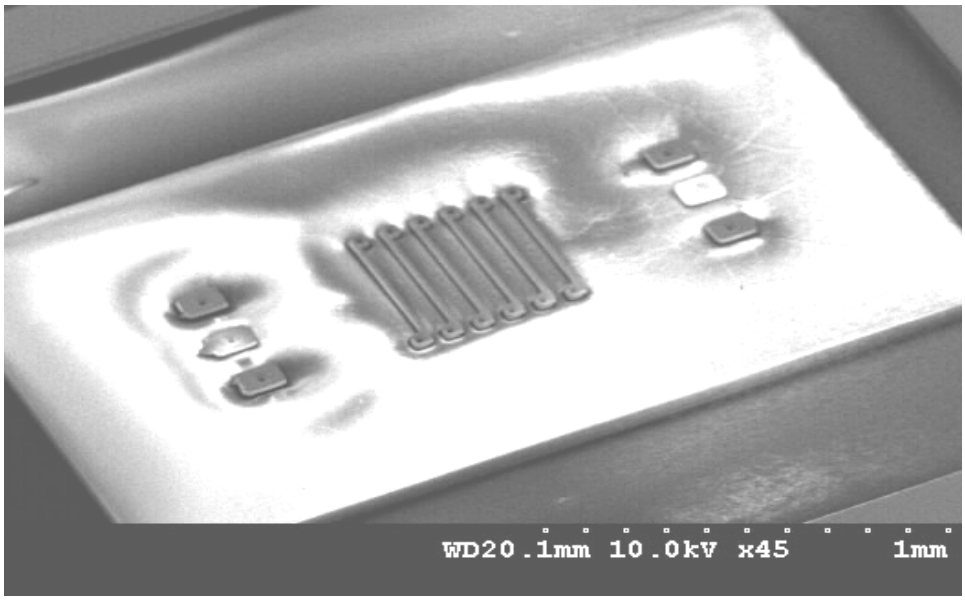
(b)



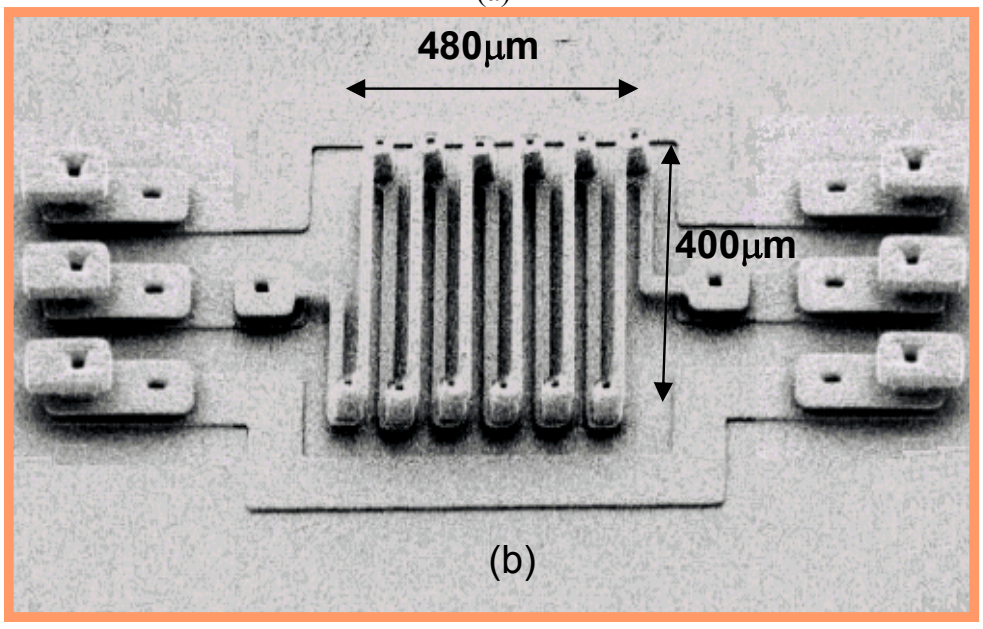
(c)

***Figure 5.3.*** *Photomicrograph of fabricated inductors: (a) A set of inductor library; (b) Top view of a six turn inductor; (c) Oblique view of a six turn inductor.*

*s)* is 80 μm, and the height of the solenoid core $h_c$ *(= h+ t)* (i.e., the distance between the center of the lower metal layer of the coil and the center of the upper metal layer of the coil) is 50 μm. The via has a cross-section of 25 μm × 30 μm.




(a)




(b)

***Figure 5.4.*** *SEM images of the fabricated 6-turn embedded test inductor: (a) Embedded; (b) After removal of SU-8.*

### 5.1.1.2. Test Inductor Results

S-parameter measurement is carried out in the frequency range of 100 MHz to 10 GHz using HP8510C vector network analyzer with standard air coplanar G-S-G probe tips (150 μm pitch) of Cascade Microtech's after a standard SOLT calibration. Inductance and Q-factor are extracted from the measured S-parameters.

Figure 5.5 shows the measured inductance and Q-factor of an embedded test inductor with 6 turns and a core width, $w_c$, of 400 μm. The peak Q-factor and inductance at 4.5 GHz are 20.5 and 2.6 nH, respectively. The measured data have been compared with MEMCAD simulation results for the same geometry. The inductance results of measurement and simulation are consistent up to 6 GHz.

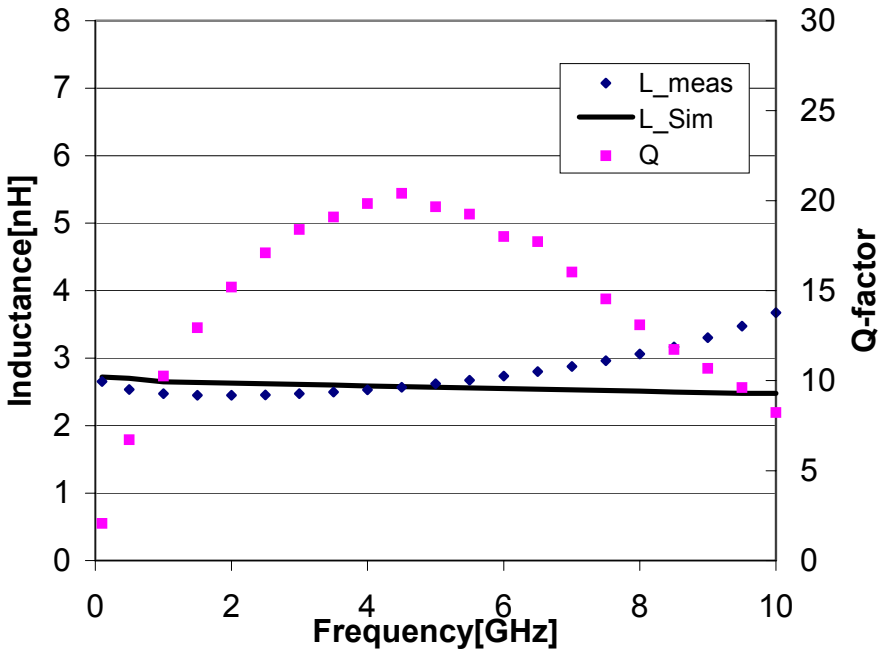



***Figure 5.5.*** *Measured inductance (diamonds) and Q-factor (squares) of an embedded test inductor (6 turns and 400 μm core width) The solid line is a simulation of the inductance using MEMCAD.*

The inductance for an ideal solenoid coil can be expressed in Equation 5.1.

$$L = N^2 \mu_c \frac{w_c h_c}{l_c} \qquad (5.1)$$

where $N$ is the number of turns, $\mu_c$ is the core permeability, $w_c$ is the core width, $h_c$ is the core height, and $l_c$ is the core length. The micromachined solenoid-type inductor is not ideal in the sense that the core is not cylindrical in shape and the wire is not wound closely enough to have the magnetic flux only inside the core. In addition, the geometric constraint of a single coil winding yields a linear relationship between pitch and core length such as $l_c = N p$. As a result, the inductance for the micromachined solenoid-type inductors can be written as Equation 5.2:

$$L = \kappa N \mu_c \frac{w_c h_c}{p} \qquad (5.2)$$

where $\kappa$ is a constant of proportionality which is determined experimentally, and the geometric substitution $l_c = N p$, where $p$ is the turn-to-turn pitch, has been made.

Figure 5.6 shows the measured inductance and Q-factor, and simulated inductance, of 6-turn inductors at 4.5 GHz as a function of core width (100 μm, 200 μm, 300 μm, and 400 μm). The inductance values calculated from Equation 5.2 are plotted with proportionality constant of 1.35, which gives good agreement with measured data. A similar analysis for number of turns is shown in Figure 5.7, with a proportionality constant of 1.25.

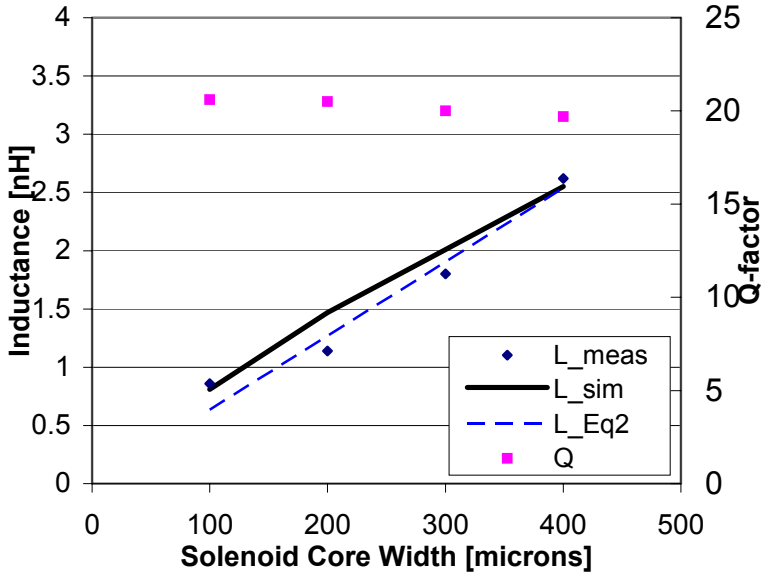



***Figure 5.6.*** *Measured inductance and Q-factor at 4.5 GHz of 6-turn embedded test inductors as a function of core width. Simulation (solid line) and Equation 5.2 (dashed line) are shown as well.*

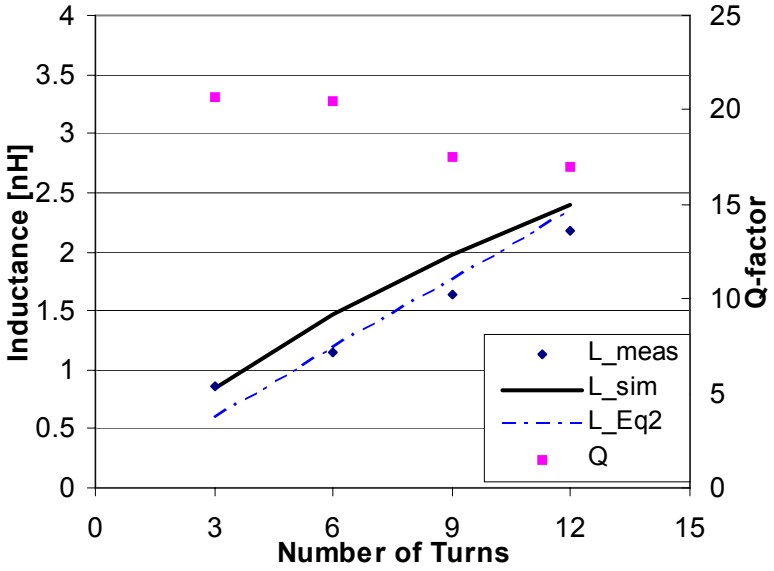



***Figure 5.7.*** *Measured inductance (diamonds) and Q-factor (squares) at 4.5 GHz of 200 μm wide embedded test inductors as a function of number of turns. The data are compared with simulation (solid line) and Equation 5.2 (dashed line).*

### 5.1.1.3. Integrated CMOS Power Amplifier Results

A CMOS power amplifier (PA) with a single-stage common-source topology was designed as a test vehicle for the embedded inductors. The schematic diagram of the amplifier is shown in Figure 5.8 [99]. The design utilizes four micromachined inductors and one integrated spiral inductor. The amplifier was fabricated using a 0.24-$\mu m$ CMOS foundry technology. The die area of the amplifier is 1,860x1,180 $\mu m^2$. Following the foundry fabrication, the four embedded micromachined inductors were fabricated on the CMOS chip as described above. Figure 5.9 shows an optical photomicrograph of the power amplifier with the integrated embedded inductors.

Figure 5.10 shows the measurement equipment and test setup for characterization of the PA which has been integrated with the micromachined inductors. Measurement was performed in the laboratory of Professor J. Laskar of Georgia Tech. An HP 8510C Vector

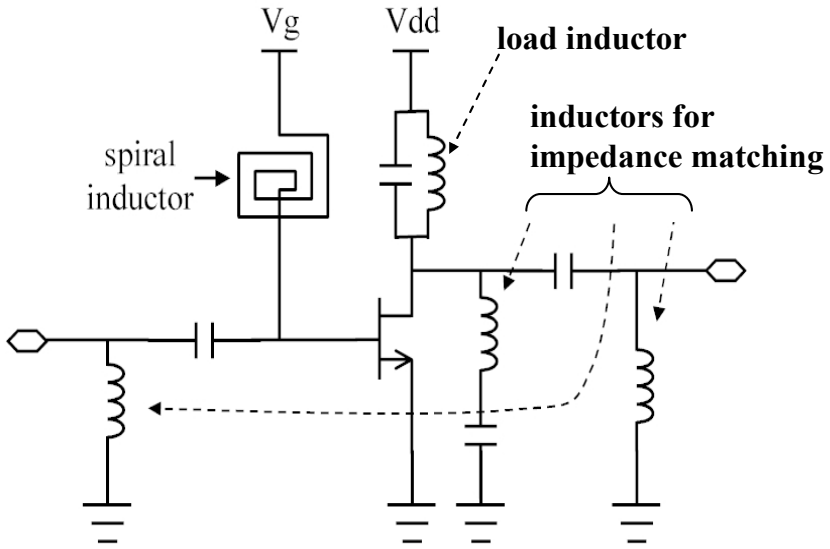



***Figure 5.8.*** *Schematic of power amplifier, showing locations of embedded inductors.*

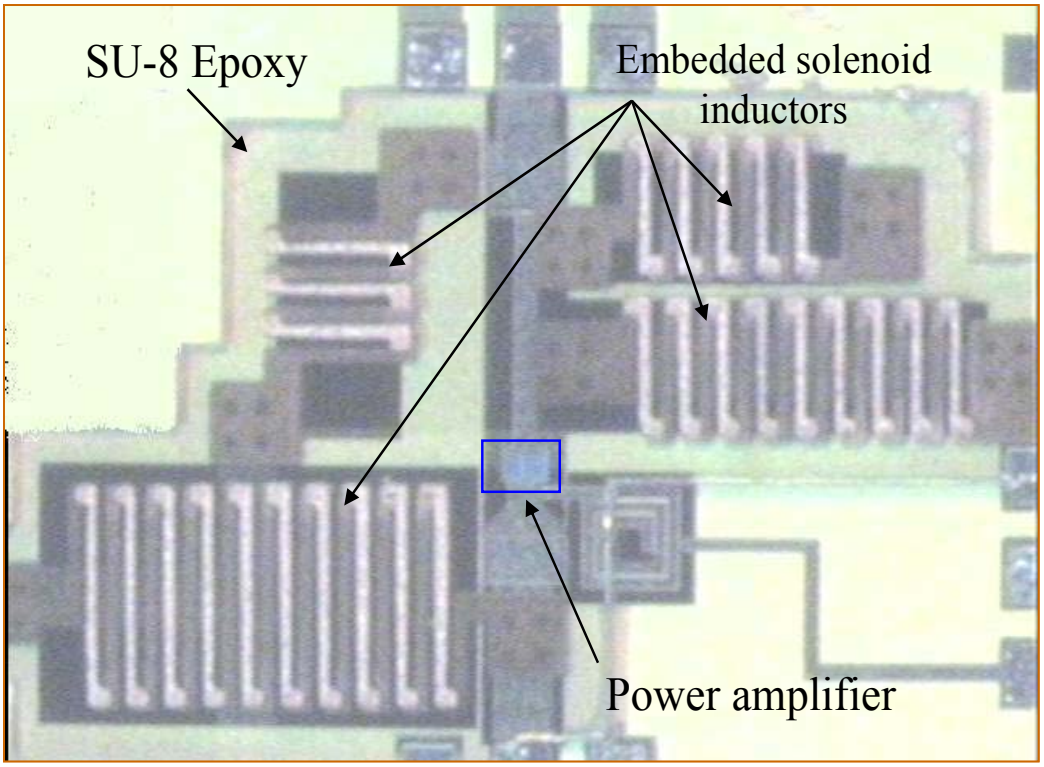
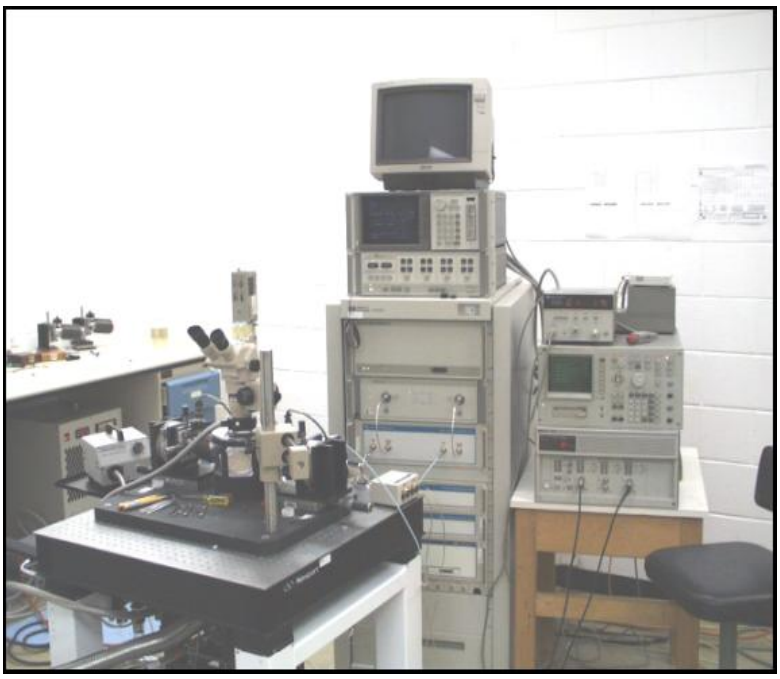



***Figure 5.9.*** *Photomicrograph of integrated power amplifier. Note the four embedded inductors.*

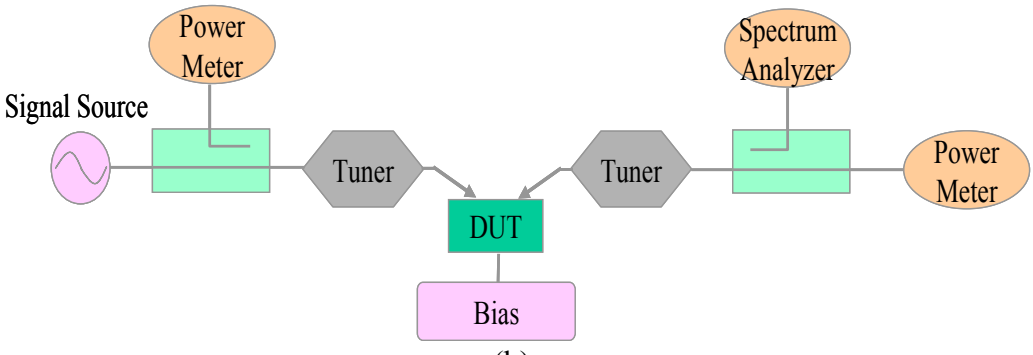
Network Analyzer, a Cascade Microtech probe station, a power supply, and a software suite comprised of HP Advanced Design Systems (HPADS) are used for the measurement and data extraction.

As the first step, a DC test to confirm functionality of the power amplifier was carried out with drain voltage $V_{dd}$ of 2.5 V and gate voltage of 1 V in Figure 5.8. A resultant drain current of 180 mA has been obtained, which is reasonable. However, when an RF input signal of 10 dBm was applied at a frequency of 2.5 GHz, a reduced maximum output power of 6.5 dBm has been obtained, resulting in negative gain. To further investigate this performance, the on-chip input matching network inductors (input and output) were opened using a laser cutter, leaving only the load inductor. In this

configuration, the amplifier was connected to external matching network. Upon a new test (Figure 5.11), the power amplifier with integrated load inductor shows a gain of 6.7 dB and a 20 % maximum power added efficiency (PAE) when it is driven at 0.8GHz, with a power supply voltage $V_{dd}$ of 2.5 V and a gate DC bias $V_g$ of 0.95 V. Even though it has not been operated at the desired frequency, these results indicated that the embedded inductor is performing successfully.

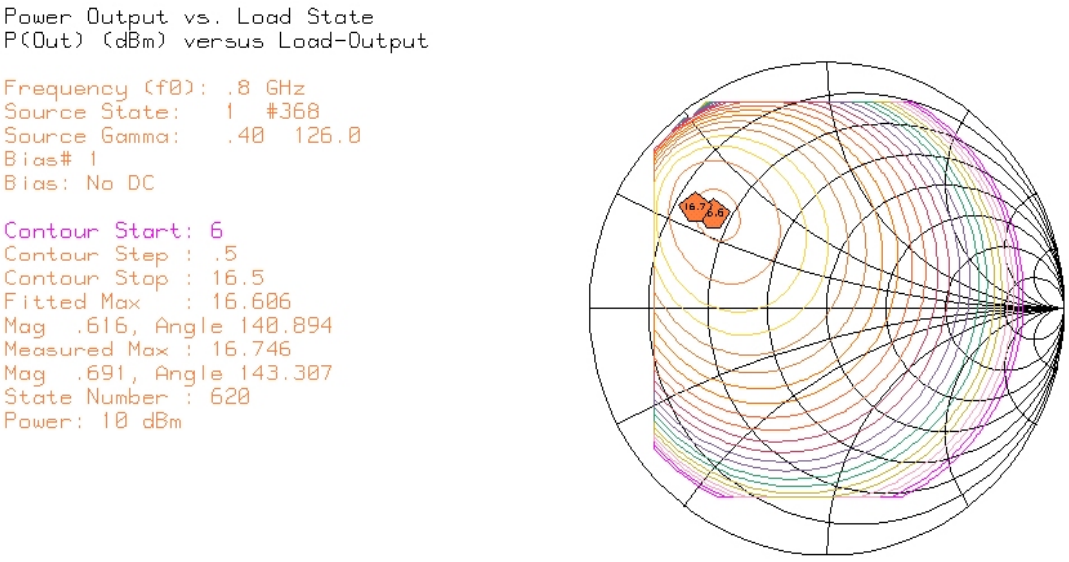


(a)

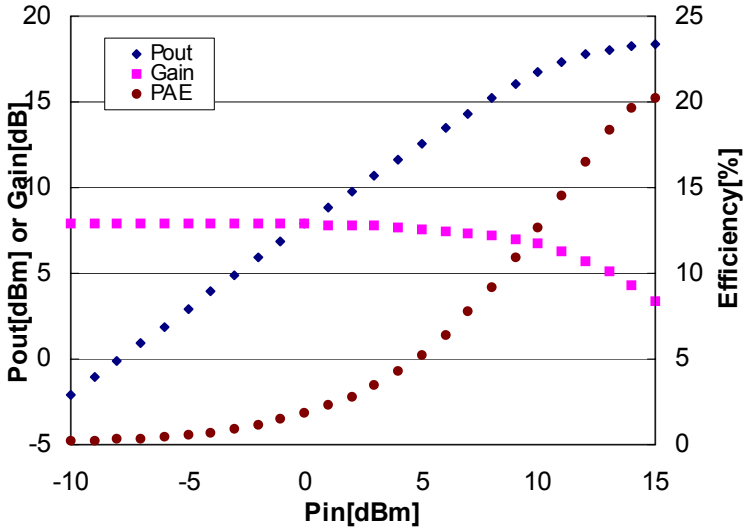



(b)

***Figure 5.10.*** *Measurement setup: (a) Equipment; (b) Test setup block diagram.*




(a)




(b)

***Figure 5.11.*** *Test results of power amplifier with integrated embedded inductors at 0.8GHz: (a) Output power vs. Load output; (b) Output power, gain, and Power Added Efficiency (PAE) of the power amplifier.*

### 5.1.2. High-Aspect-Ratio Inductor Using Epoxy Core Conductor

Most previously reported integrated 3-D RF inductors have typically been fabricated using plating through photoresist molds. However, the ratio of coil height to turn-to-turn pitch in many of these devices is relatively low due to difficulties in forming and filling extremely small, high-aspect-ratio via holes. The low profile coil suffers from magnetic flux leakage between relatively wide conductor line spaces, which can result in a decrease in Q-factor. Increased core height, leading to geometry closer to an ideal solenoid, should yield more ideal performance. In addition, the conventional integrated solenoid inductors consisted of at least three discrete layers: lower electrode, via, and upper electrode. This construction not only leads to an increased number of electrodeposition steps, but also has the potential for increased via resistance and/or mechanical weakness at each interface.

In this section, a tall high-aspect-ratio solenoid inductor is fabricated using the epoxy-core conductor technique introduced in Chapter 3. After forming a solenoid backbone structure out of SU-8 epoxy, the SU-8 backbone structure is then selectively covered in a single electrodeposition step to provide the electrical path. This column formation technique is combined with a double exposure and single development technique described in Chapter 3 to form laterally-extended bridges on top of columns. Thus, SU-8 column and bridge formation followed by metal coating is used to realize inductors with high-aspect-ratio (up to 10:1) interconnect between lower and upper conductors. With this geometry, a large inductance in the same number of turns is obtained, and the device is geometrically closer to an ideal solenoid inductor.

It should be noted that due to the skin effect, as long as the metal coating is large in thickness compared with the skin depth at the operating frequencies of interest, no degradation of conductivity is expected in epoxy-core structures compared with solid counterparts. This approach is also potentially of interest for other RF MEMS applications, such as transformers, switches, and antennas.

#### 5.1.2.1. Fabrication

The fabrication process is described in Figure 5.12. In order to selectively coat metal only on the SU-8 column, bridge, and bottom electrode definition area, three foundation layers are deposited on a glass substrate: a chromium/gold (20 nm / 100 nm thick) electrical contact layer for electroplating; a silicon dioxide (1000 nm thick) passivation layer; and a titanium/copper/titanium (Ti/Cu/Ti, 30 nm / 1000 nm / 30 nm) as a sacrificial layer for selective seed layer definition. The Ti/Cu/Ti and silicon dioxide layers are patterned for bottom electrode definition (Figure 5.12.1). A single SU-8 layer is coated and soft baked, where the thickness of the SU-8 layer becomes height of the inductor. A large optical dose is applied through the column mask and post-exposure baked at 95°C on a hot plate (Figure 5.12.2). Prior to development, a small optical dose is applied through the lateral bridge mask, and the structure is post-exposure baked at 95°C in an oven. After these two-step exposures and bakes, the SU-8 has the desired top bridge portion cross-linked at the top of the cross-linked columns (Figure 5.12.3). Developing the SU8 leaves the column and bridge. After curing the released structure in a 100°C oven for 3 hours, chromium/gold (20 nm / 150 nm) layers are coated using DC sputtering

as the seed layer for subsequent electroplating (Figure 5.12.4). Removal of the previously-deposited copper and titanium layers leaves the Cr/Au seed layers only on the surface of the SU-8 structure and the bottom electrode area. Copper/gold layers are then electroplated in sequence to a thickness of 10 - 15 microns (Figure 5.12.5). Removal of the passivation silicon dioxide and initial chromium/gold layer in sequence isolates the structure to complete the process (Figure 5.12.6).

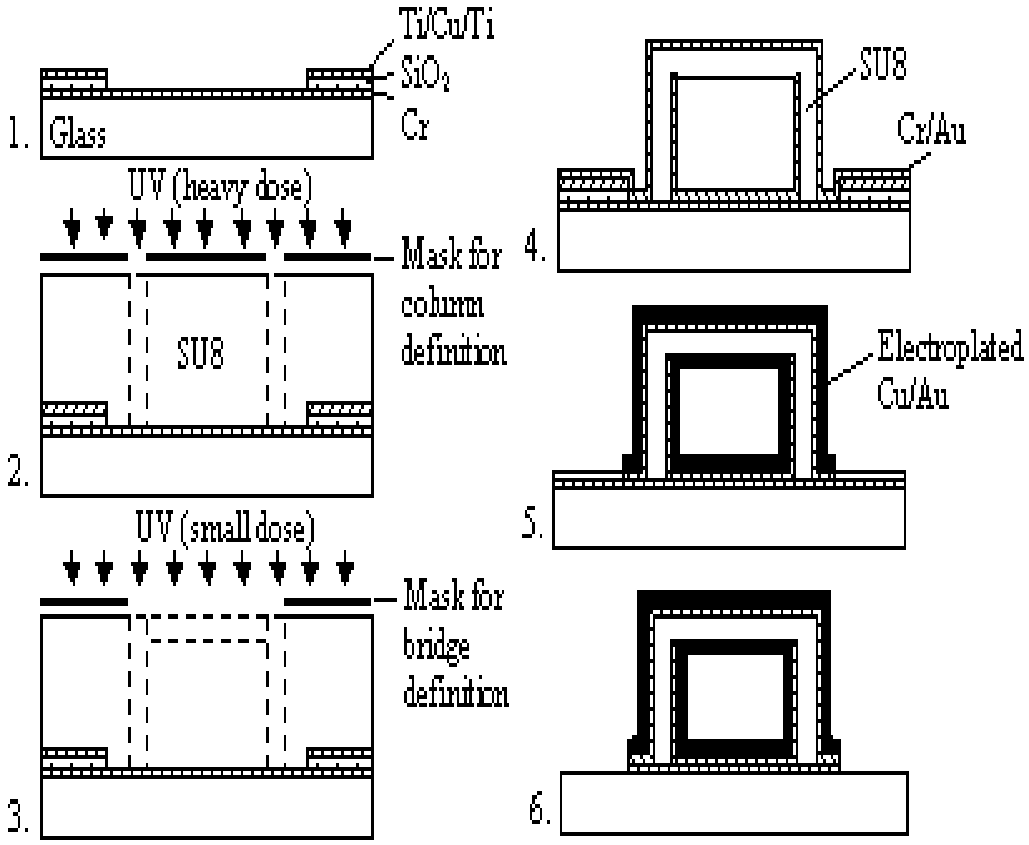
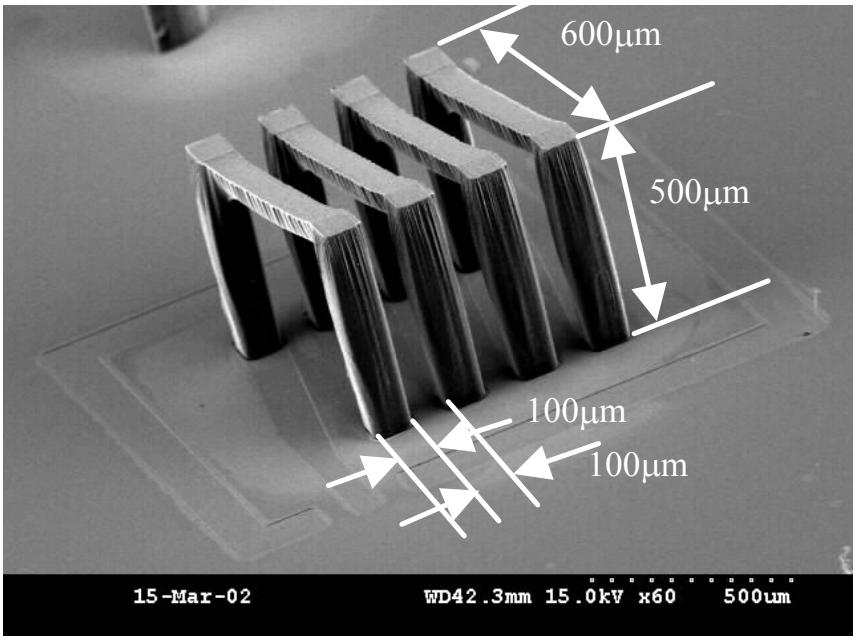



***Figure 5.12.*** *Fabrication process of high-aspect-ratio inductor using epoxy-core conductor.*

#### 5.1.2.2. Experiment and Results

Test structures are fabricated on a glass substrate. Fabricated SU-8 core structures prior to metal deposition and after metal coating to form solenoid inductors are shown in Figure 5.13a and 5.13b, respectively. The height of the inductors is approximately 0.5 millimeter and copper and gold are electrodeposited in sequence to thicknesses of 14 μm and 1 μm, respectively, in order to form electrical inductor path. Random metal bump growth through pin holes of the PECVD oxide layer has been observed on the substrate during the electroplating. These undesired metal bumps can cause some structures to be shorted. The metal bumps have been removed through an extended substrate etch in dilute HF, which may have contributed to the rough substrate surface in Figure 5.13b.

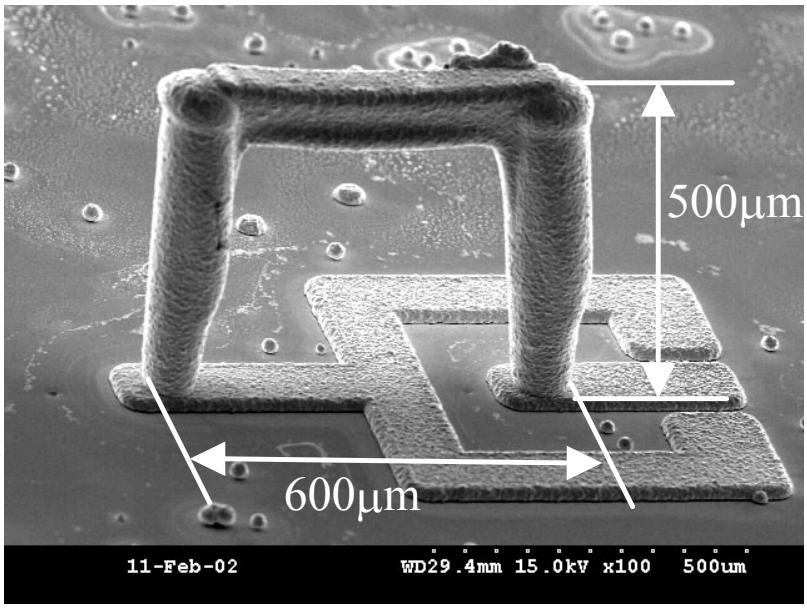
Two single-turn inductors, one 500 μm tall with a 600 μm core width, and one 900 μm tall and 600 μm in core width, are shown in Figure 5.14. S-parameter measurement is carried out in the frequency range of 100 MHz to 10 GHz using an HP8510C vector network analyzer with standard air coplanar G-S-G probe tips (150 μm pitch) of Cascade Microtech after a standard SOLT calibration. Inductance and Q-factor are extracted from the measured S-parameters. The obtained inductance and Q-factor as a function of frequency is shown in Figure 5.15. The 900 μm device shows an inductance and a maximum Q-factor of 1.17 nH and 84 (at 2.6 GHz), respectively, while the 500 μm device shows an inductance and a maximum Q-factor of 0.77 nH and 85 (at 2.5 GHz), respectively. The relatively large Q-factors indicate that the RF performance of these devices is not degraded by conductors with epoxy cores as compared with solid cores.



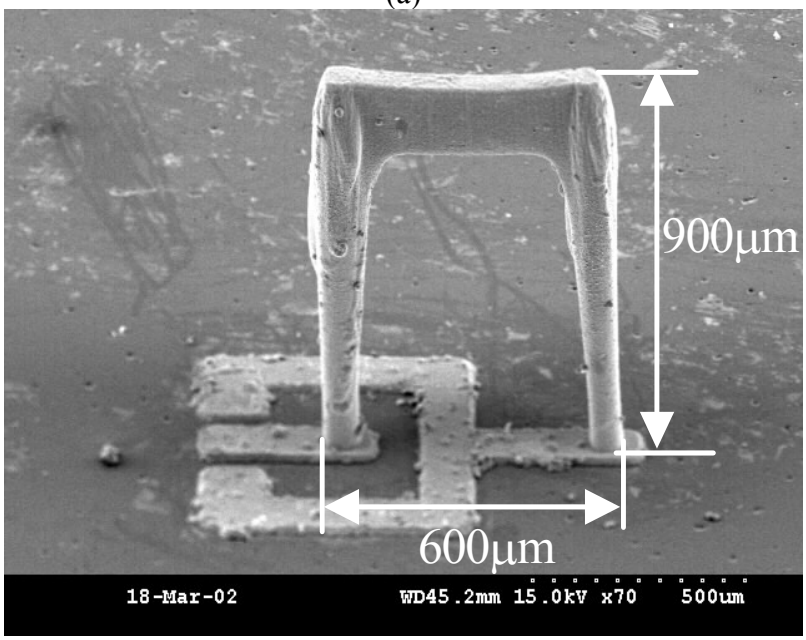

(a)


(b)

***Figure 5.13.*** *Fabricated structure: (a) Fabricated SU-8 core structures prior to metal deposition; (b) After metal coating to form solenoid inductors. Note that the height of the inductors is approximately 0.5 millimeter.*




(a)




(b)

***Figure 5.14.*** *Single turn inductors: (a) 500μm device; (b) 900μm device.*

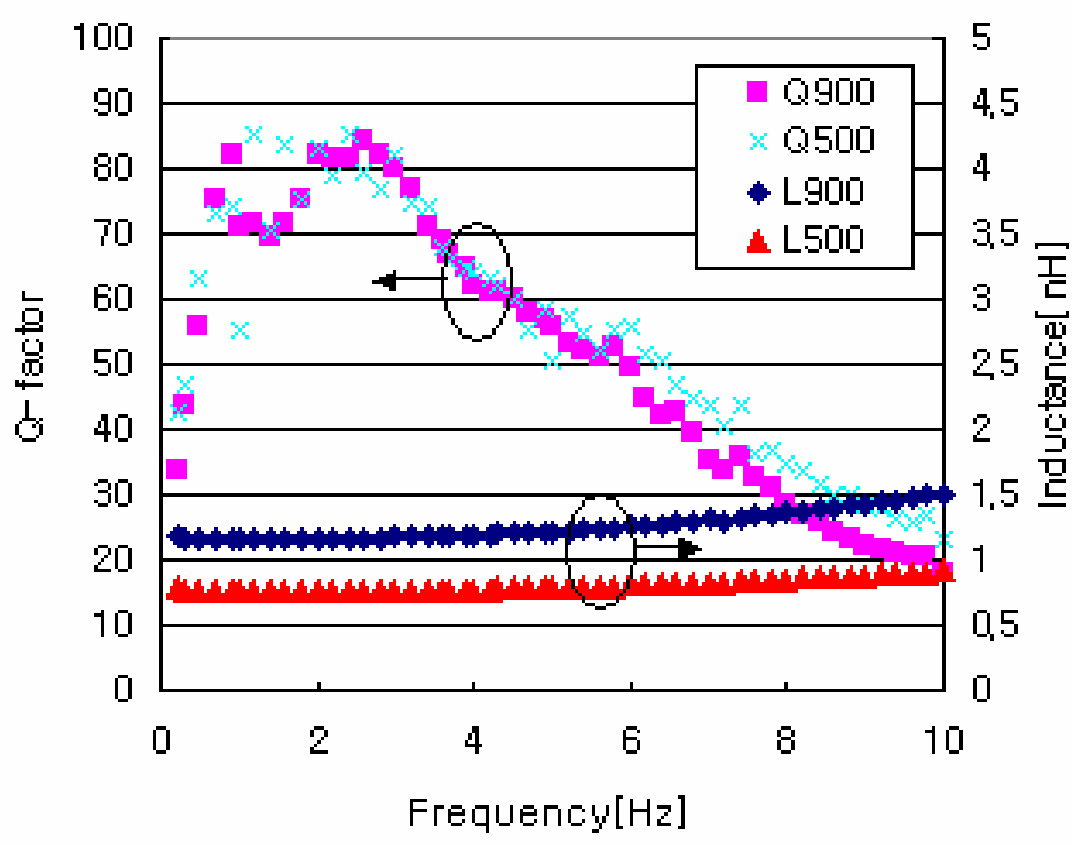



***Figure 5.15.*** *Inductance and Q-factor for two single turn inductors.*

## 5.2. RF Tunable Capacitors

While research for ferroelectric materials has progressed over last century, it is quite recently that thin-film ferroelectric materials have begun to be used for practical RF applications [100, 101]. Among various ferroelectric materials, barium strontium titanate, $Ba_{1-x}Sr_xTiO_3$ (BST), is a very attractive RF tunable material due to its large field-dependent permittivity, high dielectric constant, large breakdown voltage, and relatively low loss tangent. In addition, variable capacitors created from this material have no junction noise and have no preferred polarity compared to semiconductor varactor diodes [34, 35]. By using these advantageous properties of BST, a number of advanced high frequency tunable capacitors have been successfully demonstrated and integrated into RF components, such as phase shifters and RF filters [32, 36, 102, 103].

In this section, a simple narrow gap ferroelectric capacitor and a reduced intermodulation distortion (IMD) capacitor are designed and implemented.

### 5.2.1. BST Gap Capacitor with Low-Loss Conductor [73]

As for the ferroelectric material deposition, there are several methods reported (RF sputtering, MOCVD, CCVD, sol-gel, or pulsed laser ablation etc.) [34, 43-45, 105] and the electrical properties of tunable devices are known to vary with each method. In addition, since gap capacitors are finalized with metallization and photolithography-based patterning steps, the electrical performance of an interdigitated gap capacitor is dependent on the electrode patterning and its geometry. In this thesis, the material deposition

approach is fixed, and emphasis is placed on optimal metallization architectures and approaches to obtain improved electrical properties of the gap capacitor.

Because dielectric tunability of a ferroelectric capacitor increases with electric field, small gaps between electrodes are necessary for high tunability for a given bias voltage. A thick electrode is, also, preferred for reducing RF conductor loss. However, it is often difficult to fabricate tall and narrow gap electrodes, due in part to the general difficulties of high aspect ratio photoresist mold formation with required pattern resolution. Therefore, a critical challenge in the fabrication of these same-surface interdigitated electrodes is maintaining narrow gaps for high tunability, while simultaneously forming thick electrodes to minimize RF loss.

In this section, we describe the fabrication of a highly-tunable capacitor based on barium strontium titanate (BST:$Ba_xSr_{1-x}TiO_3$) ferroelectric thin films which have been epitaxially grown on transparent sapphire substrates. A single mask process and a repeatable self-alignment technique using reverse side exposure through the transparent substrate introduced in Chapter 3 are employed to achieve both narrow gaps and thick electrodes. An additional benefit of the process is that the BST is passivated from aggressive processing conditions, thereby maintaining its properties.

#### 5.2.1.1. Fabrication

Figure 5.16 shows a structural schematic of an interdigitated gap capacitor architecture. Two electrodes with thickness $t_e$ and gap $g$ are placed on top of high dielectric constant ferroelectric BST on sapphire substrate. The gap $g$ needs to be small

for high tunability with given bias voltage and is targeted to 1~2 μm in width. To reduce RF conductor loss, the electrode thickness $t_e$ is targeted to be 2 μm, which is about one skin depth of copper at 1 GHz. The fabrication process follows in Figure 5.17. BST is grown to a thickness of approximately 0.5 μm thick on single-crystal alumina sapphire substrates using combustion chemical vapor deposition (CCVD) at nGimat, Inc. This technique allows epitaxial growth of BST in non-vacuum conditions. Negative tone photoresist (NR9_100PY, Futurrex, Inc.) is spin-coated on the BST film and patterned. In a lift-off process, first metal layers (Cr/Cu/Au, 200 Å / 2000 Å / 150 Å) are deposited and the photoresist removed (a). Chromium is used as an adhesion layer between the substrate and the subsequently-deposited copper layer, and the top gold layer is for oxidation protection. A second negative photoresist (NR9_1500, Futurrex) is then spin-coated and baked. The photoresist is then exposed from the reverse side. Since the sapphire substrate

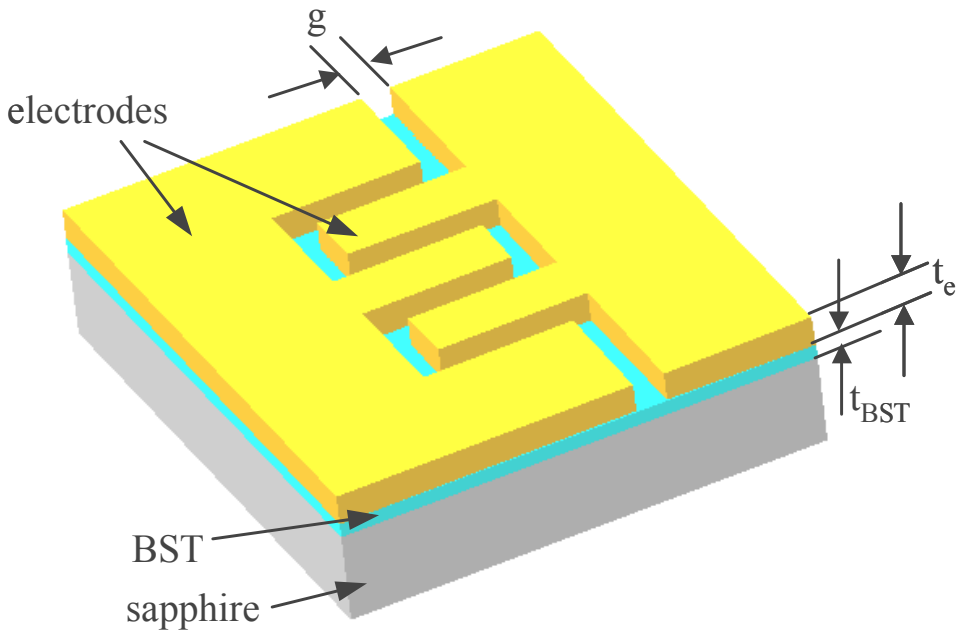



***Figure 5.16.*** *Structural schematic of an interdigitated gap capacitor on barium strontium titanate (BST) on sapphire substrate.*

is transparent, a negative photoresist is used, and since the first metal layer is opaque, a self-aligned mold is opened over the first deposited metal layer (b). This mold can then be filled either using electroplating or subsequent lift-off steps to create thick, self-aligned electrodes. In this work, multiple lift-off processes are employed. Ti/Cu/Au (100 Å / 8000 Å / 150 Å) is deposited using a standard lift-off process followed by photoresist removal (c). A third metallization and lift-off has been done for further metal thickness and the fabrication is complete (d).

A fabricated single digit gap capacitor with 300 μm coupling length is shown in Figure 5.18a, yielding 1.2 μm gap and 0.2 μm thickness after the first lift-off (Figure 5.18b), and 1.2 μm gap and 2.2 μm thickness (1.8:1 gap aspect ratio) after the third lift-off process (Figure 5.18c).

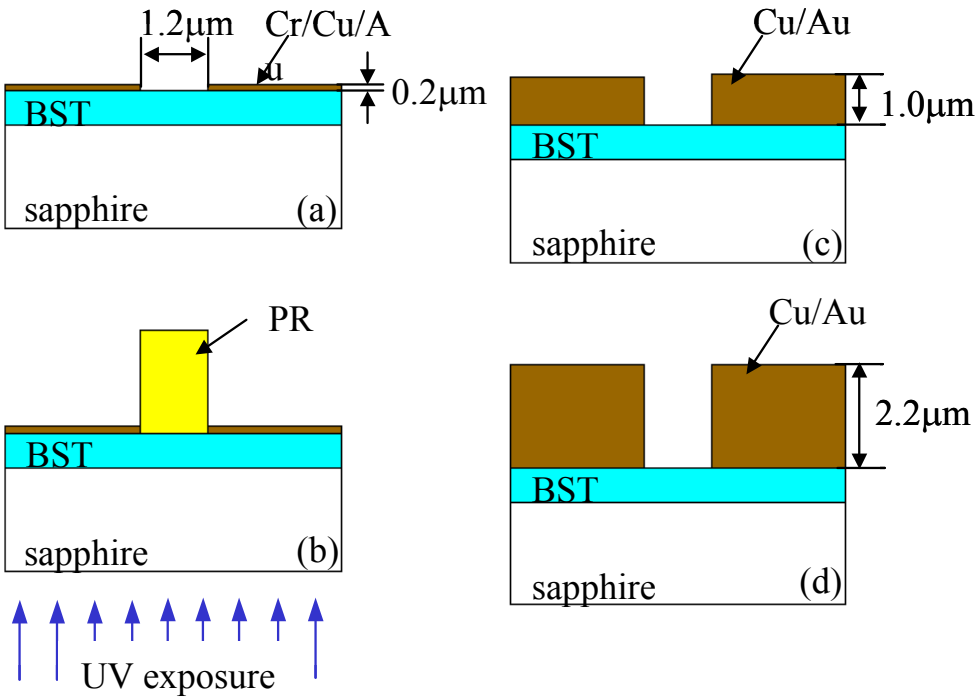



***Figure 5.17.*** *Fabrication process.*

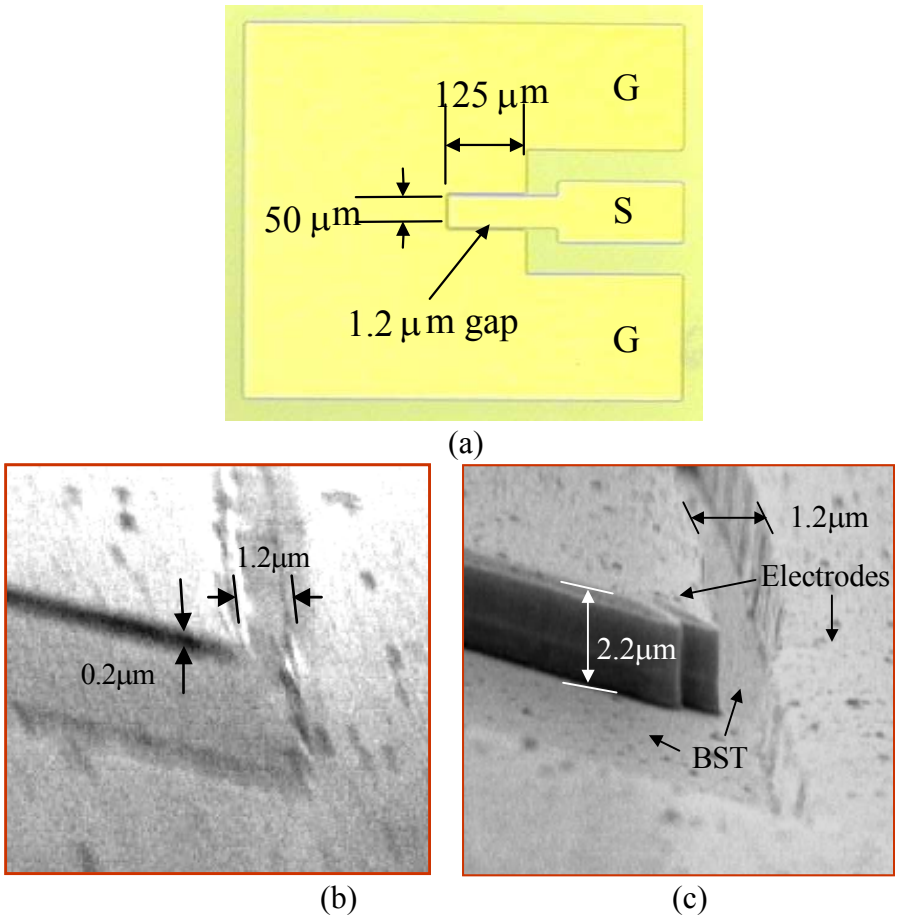



***Figure 5.18.*** *A fabricated single digit gap capacitor: (a) 1.2 µm gap and 300 µm coupling length; (b) SEM picture of gap area after the first lift-off (0.2 µm thick metal); (c) After the third lift-off (2.2 µm thick metal).*

#### 5.2.1.2. Capacitance as a function of Bias Voltage

Impedance for the fabricated gap capacitors is measured with Keithley 3322 LCZ meter at 100 kHz. The capacitance and its tunability as a function of dc bias voltage for the capacitor of Figure 18a (2.2 µm thick electrodes) are plotted in Figure 19. The capacitance is decreasing with positive bias voltage and showing hyperbolic curve dependence ($C \propto 1/V$). Since capacitance of a gap capacitor is insensitive to the polarity

of the bias voltage, it is axisymmetrically plotted to the y-axis. Voltage dependent capacitance *C(V)* and tunability *T(V)* ($T=100\times(C_0-C_{bias})/C_0$) can be expressed as Equation 5.3 and 5.4, respectively.

$$C(V) = C_{os} + \frac{k}{|V| + V_{os}} \tag{5.3}$$

$$\begin{aligned} T(V) &= \left| \frac{C(0) - C(V)}{C(0)} \right| \times 100 \\ &= \left| 1 - \frac{C_{os}}{C(0)} - \frac{k / C(0)}{|V| + V_{os}} \right| \times 100 \end{aligned} \tag{5.4}$$

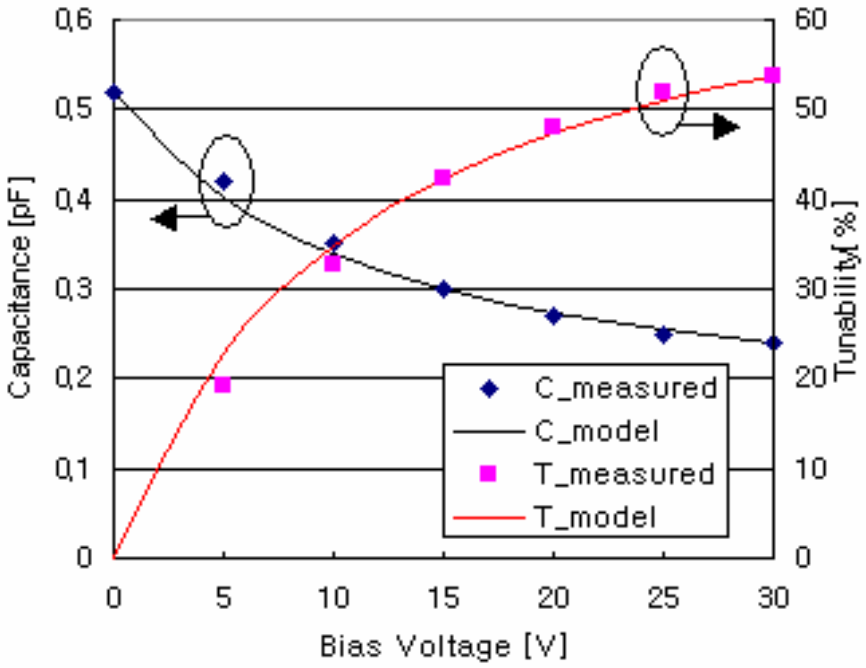



***Figure 5.19.*** *Capacitance and tunability of a single digit gap capacitor structure (1.2 μm gap and 300 μm coupling length).*

where $C_{os}$ is non-voltage dependent offset capacitance, $k$ a coefficient of the hyperbolic function, $|V|$ the magnitude of the biasing voltage, and $V_{os}$ an offset voltage to give a finite capacitance value at zero bias voltage.

The coefficients ($C_{os}$, $k$, and $V_{os}$) are empirically determined with the measurement data from at least three different voltages. Capacitance and tunability from Equations 5.3 and 5.4 for the device shown in Figure 5.18a are also plotted in Figure 5.19. Modeling curves show good agreement with the measurement data through all the voltage range (0~30V). The coefficients used for the plot are summarized in Table 5-1.

**Table 5-1.** Coefficients for capacitance and tunability curves

| | $C_{os}$ [pF] | k [pF• V] | $V_{os}$ [V] |
|---|---|---|---|
| Capacitor in Fig. 5.18a | 0.135 | 4.33 | 11.24 |

#### 5.2.1.3. Capacitance according to Gap

Since a gap capacitor fabricated on a high dielectric layer is storing electric energy mostly in the dielectric beneath the gap area, its capacitance is heavily dependent on the fringing field between the electrodes through the dielectric. A capacitance formula is not easy to obtain in a simple analytic form from the geometrical dimension and its dielectric constant as can be done for a parallel capacitor. The capacitance for a gap capacitor, however, over a limited range of geometry, might be formulated in Equation 5.5 (which mimics the functional form of a parallel capacitor), if appropriate constants of proportionality can be determined.

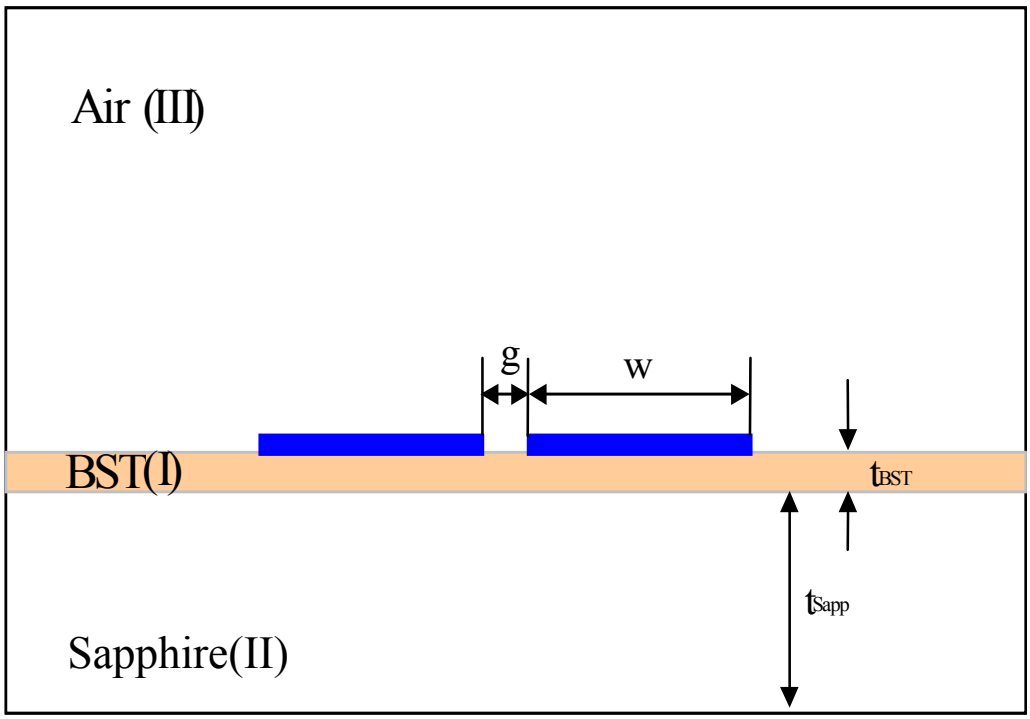



***Figure 5.20.*** *Capacitor geometry for 2-D electric analysis.*

$$C(g) = \varepsilon_0 \varepsilon_r \frac{\alpha \cdot t}{g^{\beta}} \qquad (5.5)$$

where $\alpha$ is an effective coupling length, $t$ the thickness of the dielectric layer, $g$ the gap between the electrodes, and $\beta$ an effective power factor.

A finite element analysis (ANSYS 5.6) is used in order to numercally determine $\alpha$ and $\beta$ for a given capacitor geometry,. The geometry used for two dimensional electrostatic simulation is shown in Figure 5.20 and the parameters used are as follows.

Relative permittivity of air $\varepsilon_{air}$ : 1

Relative permittivity of sapphire $\varepsilon_{sapp}$ : 10

Relative permittivity of BST $\varepsilon_{BST}$: 800

Thickness of BST $t_{BST}$ : 0.5 μm

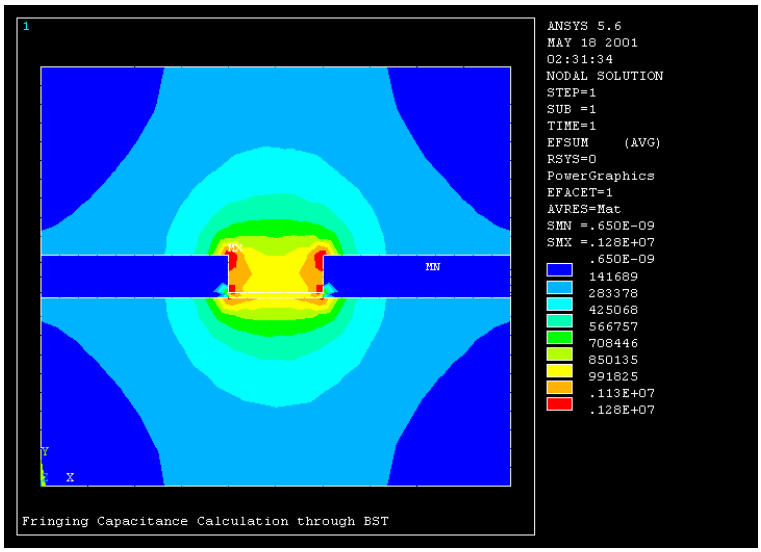
Width of electrode $w$ : 500 μm

Gap $g$ : 0.5 μm ~ 20 μm

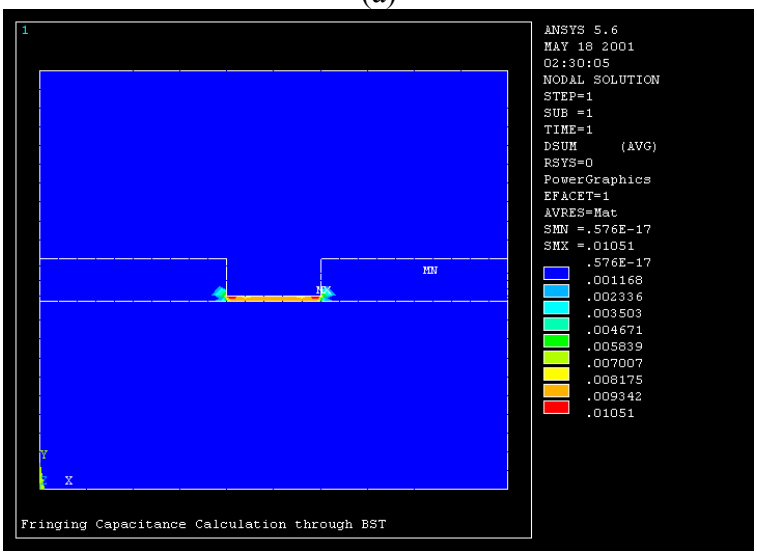
Electric field and electric displacement in the gap area are shown in Figure 5.21. While strong electric field is concentrated on the gap area symmetrically between electrodes regardless of upper air region and underneath substrate region in Figure 5.21a, strong electric displacement is displayed only in the high dielectric BST layer of the gap area in Figure 5.21b. More than 80% of the total stored electric energy between the electrodes is attributed to that area.

Also, several capacitors with various gaps (1.2 μm, 2.5 μm, 5 μm, 10 μm, and 20 μm) have been fabricated and their impedance measured at zero and 30 volt DC bias. Figure 5.22 shows the capacitance and tunability as a function of the gap. A solid line, square marks, and diamond marks represent the simulated capacitance with zero bias voltage, measured capacitance with zero bias, and measured capacitance with 30 V, respectively. Note that the fabricated samples have their capacitance converted to capacitance per unit length (pF/mm) in comparison with simulation results. The solid curve in Figure 5.22 is a best fit in Equation 5.6.

$$C(g) = \frac{2.531}{g^{0.782}} \text{ [pF/mm]} \qquad (5.6)$$




(a)




(b)

***Figure 5.21.*** *Magnified view of electric field and electric displacement distribution in gap area with 5μm gap: (a) Electric field ($|\bar{E}|$); (b) Electric displacement ($\varepsilon|\bar{E}|$) (ANSYS 5.6).*

where $g$ is in a μm unit. By comparison of Equation 5.5 and 5.6 with proper unit conversion, $\alpha$ and $\beta$ are determined to be 0.714 m and 0.782, respectively.

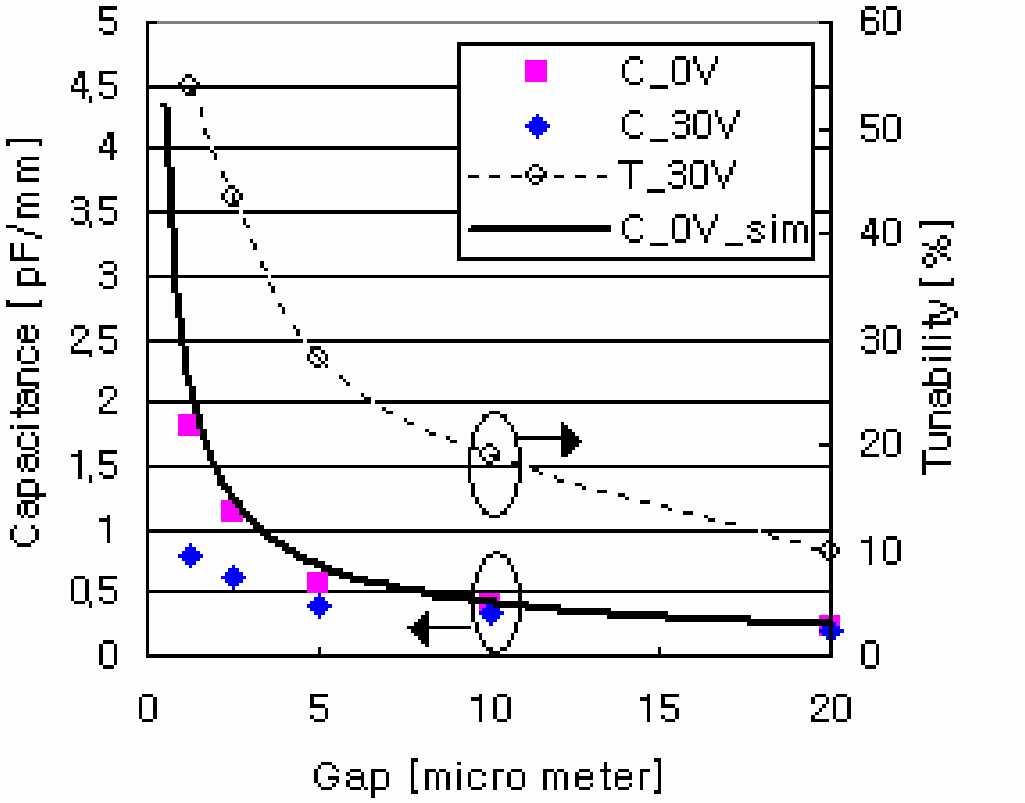



***Figure 5.22.*** *Capacitance and tunability according to gap: Filled squares and diamonds show measured capacitance, the solid line is simulated capacitance, and the dashed line with empty circles is measured tunability at 30V.*

It is observed that a capacitor with a narrower gap shows a larger value than that of a wider gap, and its percent change for a given bias voltage shows a similar trend as well. Large tunability benefits from a narrow gap as expected.

#### 5.2.1.4. Q-factor

In general, all practical passive components (R, L, and C etc.) are not ideal and can be modeled as a combination of complex impedances with unwanted parasitics. As for a

capacitor, the practical model includes unwanted inductance, resistance, and dielectric absorption. A typical practical model is schematically drawn as in Figure 5.23, where $C$ is the ideal capacitance, $R_p$ the parallel resistance representing dielectric loss, $R_{esr}$ the equivalent series resistance, and $L_s$ the series parasitic inductance.

The total impedance is written in Equation 5.7

$$Z = \mathrm{Re}(Z) + j\,\mathrm{Im}(Z) \tag{5.7}$$

where

$$\begin{aligned} \mathrm{Re}(Z) &= \frac{R_p + R_{esr} + \omega^2 C^2 R_p{}^2 R_{esr}}{1 + \omega^2 C^2 R_p{}^2}, \\ \mathrm{Im}(Z) &= \frac{-\omega C R_p{}^2 + \omega L_s + \omega^3 L_s C^2 R_p{}^2}{1 + \omega^2 C^2 R_p{}^2} \end{aligned} \tag{5.8}$$

The quality factor Q is defined as the ratio of the energy stored in the device to energy dissipated per cycle. It is easily calculated for the passive components as shown in Equation 5.9 if complex impedance is known.

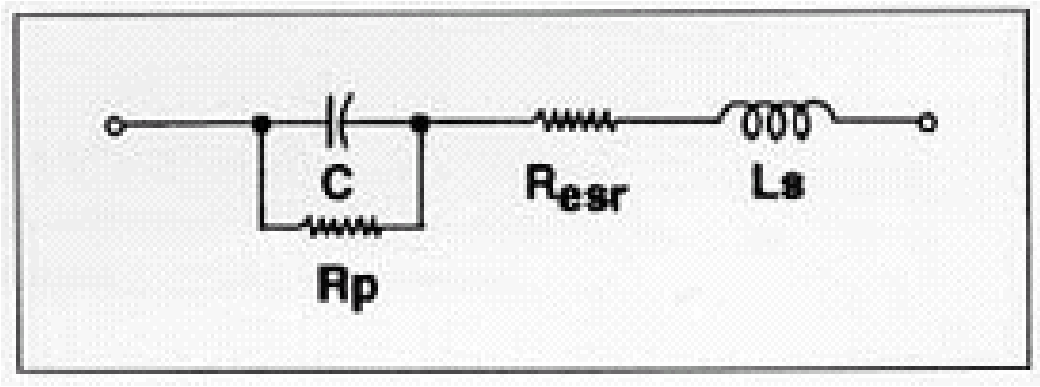



***Figure 5.23.*** *Equivalent circuit for a gap capacitor.*

$$Q = -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \qquad (5.9)$$

In the high frequency region, the real part of the impedance *Re(Z)* is dominated by $R_{esr}$ while the imaginary part *Im(Z)* is approximated to $-1/\omega C$ as long as the operating frequency is below its self-resonant frequency. Therefore, the high Q-factor can be achieved by suppressing its equivalent series resistance $R_{esr}$ existing in the radio frequency of interest.

Equivalent series resistance $R_{esr}$ in the RF range consists of DC resistance, RF resistance, and contact resistance, etc. DC resistance and metal contact resistance are independent of frequency whereas RF resistance is a frequency dependent function due to

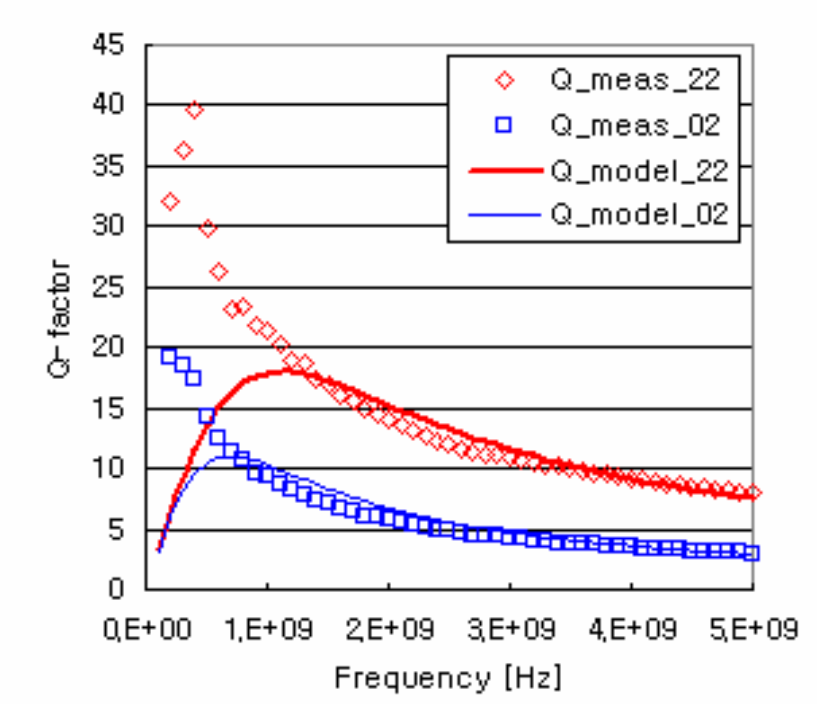



***Figure 5.24.*** *Quality factor of gap capacitors with two different metal thicknesses: Diamonds and squares represent q-factors for 2.2 μm thick capacitor and 0.2 μm thick one, respectively.*

the skin effect at high frequency. In order to minimize its RF resistance, the conductors for RF devices are designed to be at least as thick as its skin depth in the frequency of interest. A thicker conductor than several skin depths does not have much benefit, if any, from its thickness at the costs of fabrication difficulty for thick conductor structure since the portion of the conductor much deeper than the skin depth contains very little current at high frequency.

The skin depth of copper at 1 GHz is approximately 2 μm and the copper electrodes for the test gap capacitors are 2 μm thick or thicker. Two gap capacitors (one with 0.2 μm thick electrodes and the other with 2.2 μm thick ones) have been tested in the frequency range between 100 MHz and 5 GHz to investigate the effect of electrode thickness on Q-factor.

One-port scattering parameters are taken using the HP 8510 Vector Network Analyzer and Cascode G-S-G probe systems after its standard calibration. S-parameters are converted to Z- parameters and the Q-factors are calculated using Equation 5.9. The resultant data are plotted in Figure 5.24, where the square marks and the diamond marks represent Q-factor of 0.2 μm thick capacitor and 2.2 μm thick, respectively.

By fitting Q values from Equation 5.8 and 5.9 to those from measurement in 1 GHz through 5 GHz (solid lines in Figure 5.24), lumped parameters in Figure 5.23 are determined and summarized in Table 5-2. The equivalent series resistance $R_{esr}$ for the 2.2 μm device is smaller than that of the 0.2 μm one, resulting in Q-factor improvement.

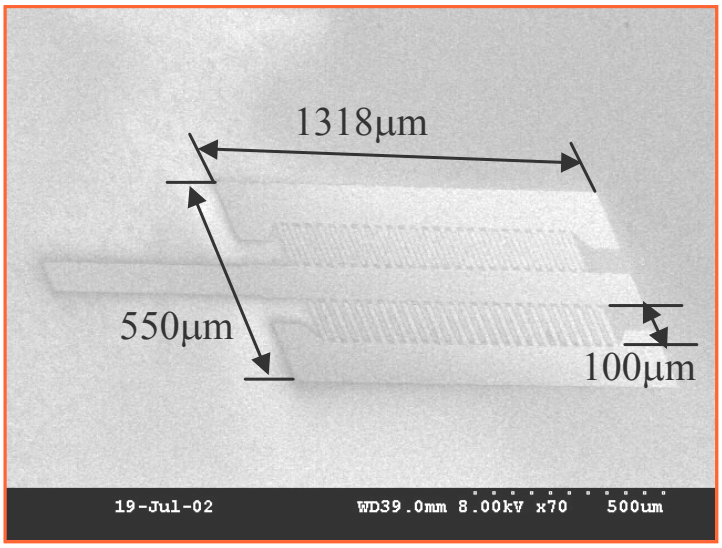
#### 5.2.1.5. Multi-interdigitated Capacitor

Based on the initial test structures above, a 102-finger interdigitated capacitor has been fabricated to demonstrate the feasibility of the proposed process for large capacitance with multi-interdigitated structure. Later, this structure is embedded in SU-8 epoxy for passivation and tested.

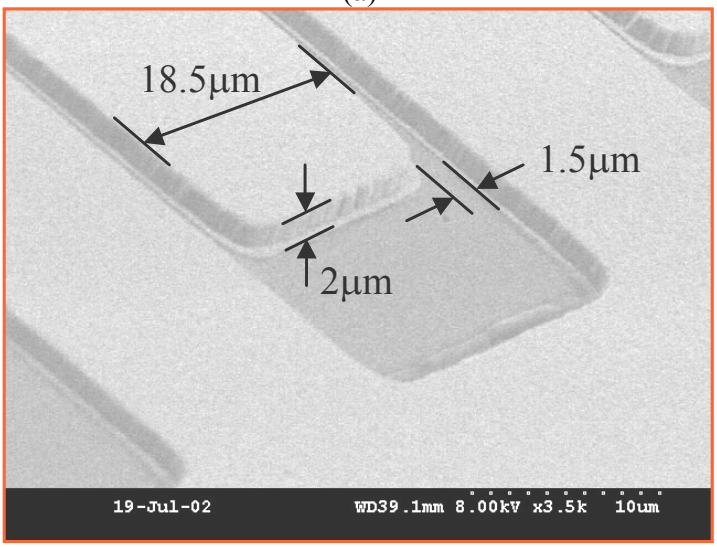
Since the thick conductor process uses a self-alignment technique, the multiple interdigitated structure does not introduce any additional process complexity. The capacitor is a coplanar waveguide type gap capacitor having 51-finger electrodes 100 μm long, 18 μm wide, and 2 μm thick between signal conductor and each ground conductor (Figure 5.25 shows SEM pictures of capacitor before it is embedded in SU-8). The overall dimension of the capacitor is 1318 μm x 550 μm and the gap is 1.5 μm.

The structure is embedded in a 25 μm thick SU-8 epoxy layer for passivation with a pad opening for the probe. Before embedding, this capacitor shows 17.8 pF, 33 % tunability at 10 V, and a quality factor of 46 (at 10 V bias) in Figure 5.26. After embedding, a slight degradation in Q-factor and tunability is observed, resulting from additional dielectric loss due to the SU-8 layer as well as non-tunable, $\varepsilon_r > 1$ SU-8 material filling the gap area. The overall capacitance slightly increased due to this additional dielectric contribution from the SU-8. The capacitor exhibits a capacitance of 18.9 pF, tunability of 32 % at 10 V, and a quality factor of 39 (at 10 V bias). All measurements in Figure 5.26 were performed at a frequency of 100 kHz.

The embedded structure has been characterized at 1 GHz for RF application. It shows 15.9 pF of capacitance, 28.1 % of tunability at 10 V, and quality factor of 16 (at 10 V bias) in Figure 5.27.




(a)




(b)

***Figure 5.25.*** *SEM images for a 102-finger interdigitated capacitor before embedding: (a) Overall view; (b) Magnified view.*

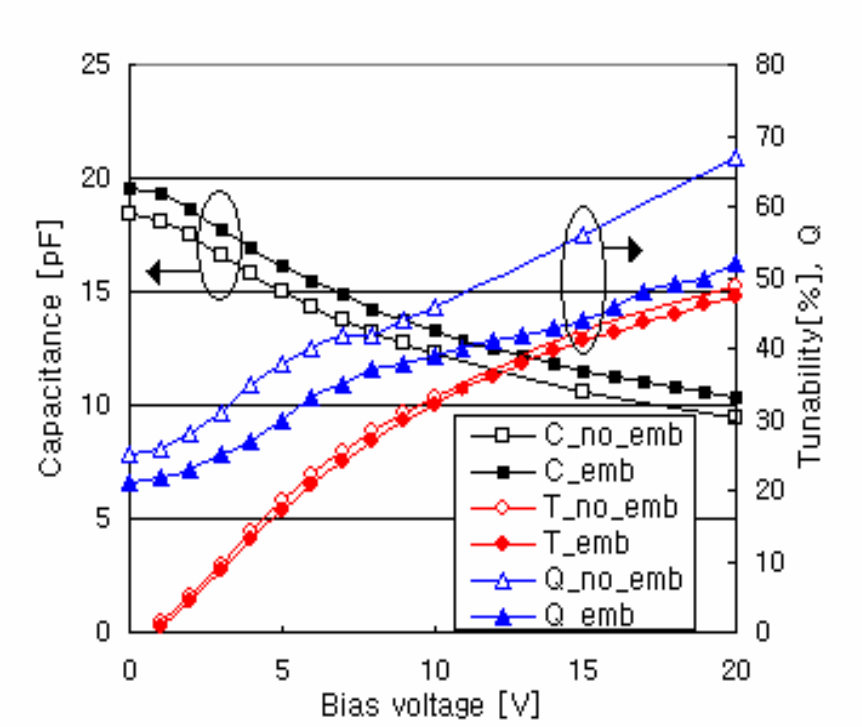



***Figure 5.26.*** *Capacitance, tunability, and Q-factor vs. bias voltage for a 102-finger interdigitated capacitor at 100 kHz.*

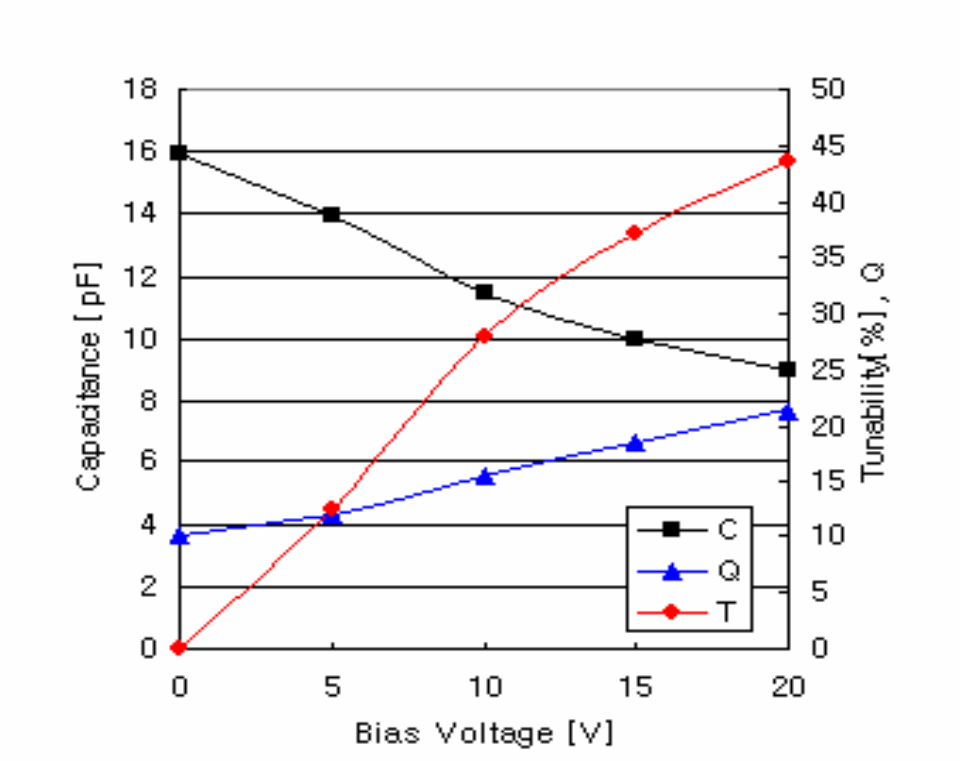



***Figure 5.27.*** *Capacitance, tunability, and Q-factor vs. bias voltage for a 102-interdigited capacitor at 1GHz.*

### 5.2.2. Reduced IMD Tunable Ferroelectric Capacitor : Part I

This section describes device implementation of a ferroelectric tunable capacitor based on the reduced IMD architecture introduced in Chapter 4. The capacitor has an additional, highly resistive DC bias structure constructed within the RF gap capacitor. In this section, Part I, the discussion is focused on the proof of concept for the reduced IMD architecture. In Part II, the discussion is extended to an IMD improvement scheme with a wide RF gap and multi-pair DC bias electrodes.

#### 5.2.2.1. Fabrication

For device concept verification and performance comparison, the five types of gap capacitors mentioned in Chapter 4.1 and in Table I (type I ~ type V) are fabricated with RF electrodes of 1~2 μm thickness and 12~14 μm RF gap, and DC bias electrodes of 1~2 μm spacing and 2~3 μm electrode width. Oxide electrodes, such as indium tin oxide (ITO) or lanthanum strontium cobalt oxide (LSCO) of 3~10 nm thickness, are used for the high resistivity DC bias electrodes. The sheet resistance of these films is in the range of $2\sim3\times10^4$ Ω/sq. Alternate highly resistive materials, such as lightly doped silicon or polysilicon, could also be utilized.

Figure 5.28 shows two fabrication processes utilized in the realization of the reduced IMD capacitors. Figure 5.28a shows two sequential lift-off processes; the first for definition of the high resistivity bias electrodes, and the second for definition of the high conductivity RF electrodes. First, barium strontium titanate ($Ba_{0.6}Sr_{0.4}TiO_3$: BST)

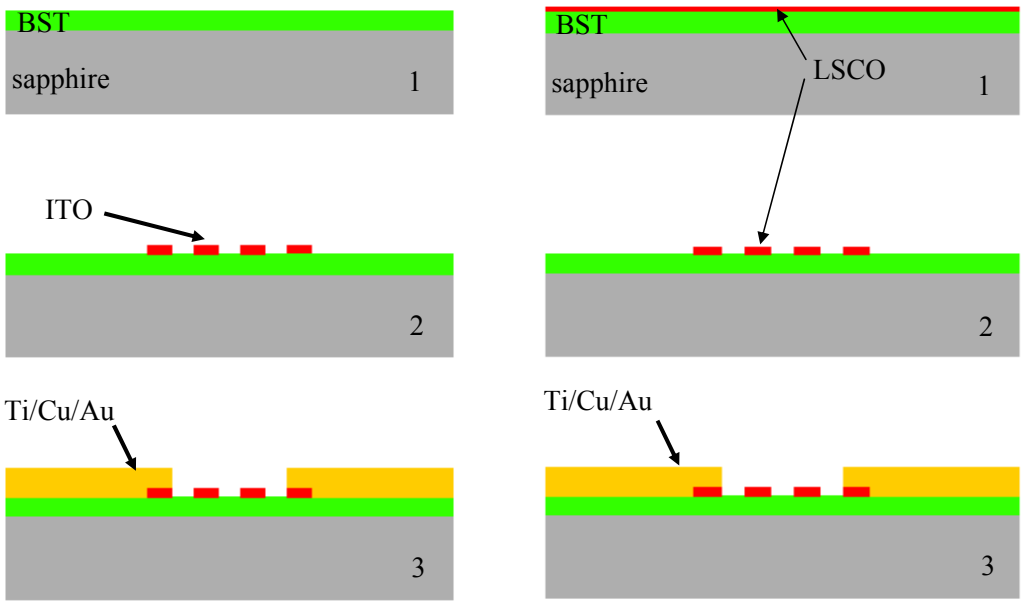
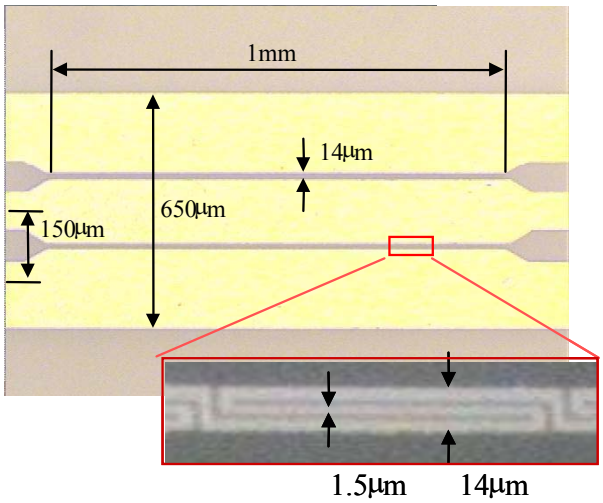
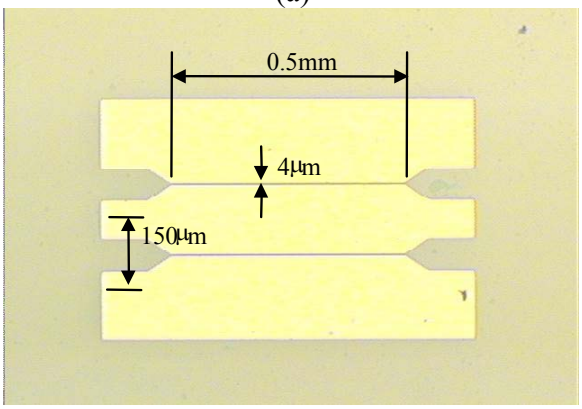



***Figure 5.28.*** *Fabrication processes for ITO and LSCO electrode reduced IMD capacitors: (a) 1. BST/sapphire substrate; 2. ITO sputter deposition and patterning using lift-off; 3. RF pad patterning using lift-off, (b) 1. LSCO/BST/sapphire substrate; 2. LSCO pattering using etching; 3. RF pad patterning using lift-off process.*

ferroelectric thin films (450 nm thick) epitaxially grown on sapphire substrates (430 μm thick) using combustion chemical vapor deposition (CCVD) [105] by Microcoating Technologies, Inc. (MCT), Chamblee, GA, are used as a starting substrate (a/1). To create the highly resistive bias structure electrodes, an indium tin oxide (ITO) layer 10 nm in thickness is deposited and patterned using RF sputtering and lift-off (a/2). The measured sheet resistance of the ITO is $2\sim3\times10^4$ Ω/sq. Lastly, the RF conductors are formed using a standard lift-off process with 1μm thick copper and 0.3 μm thick gold (a/3). Since this process is an acid-free process, it prevents the BST layer from being damaged or degraded by any corrosive acidic chemical during the process.




(a)




(b)

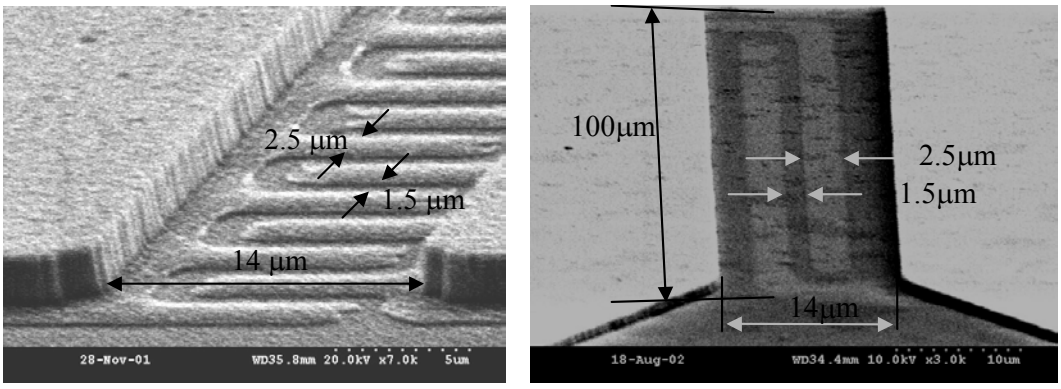
***Figure 5.29.*** *Photomicrograph of the fabricated gap capacitors with ITO bias electrodes: (a) Long ABE capacitor (type IV, 14μm RF gap, 1mm RF electrode length, 1.5μm DC bias gap, and 10 repeated bias structures), magnified unit bias electrodes in the inset (SEM picture); (b) Conventional narrow gap capacitor for IMD comparison (type II, 4μm gap and 0.5mm RF electrode length).*

One drawback of the above process is the necessity for a separate sputter deposition step for the highly resistive material. It is known that CCVD can be utilized to deposit highly resistive oxides such as ITO and LSCO. Therefore, a manufacturing advantage can be obtained if, e.g., an LSCO layer can be deposited directly on the BST by CCVD. However, since CCVD is carried out at relatively high temperature, a liftoff process using

conventional photoresists is infeasible. Therefore, a modified process requiring etching of the highly resistive material is required.

Figure 5.28b shows a fabrication process, which uses one etch and one lift-off step. Lanthanum strontium cobalt oxide (LSCO) is grown on top of the BST layer on the sapphire substrate by Microcoating Technologies using a sequential CCVD process. (b/1). Photoresist is patterned for DC bias electrode definition. LSCO is etched in dilute hydrochloric acid and the photoresist is removed (b/2). The RF conductor is formed as described above and shown in b/3.

To minimize the parasitic capacitance between signal and ground lines, a shunt capacitor scheme was adopted using a coplanar waveguide configuration. A fabricated device using ITO resistive electrodes is shown in Figure 5.29. Figure 5.29a shows a long ABE structure (type IV) with 1 mm long RF electrodes, a 14 μm RF gap, ten repeated ITO bias electrode groups with 100 μm group pitch and 1.5 μm DC bias gap. Figure 5.29b shows a conventional narrow gap capacitor (type II) with a 4 μm gap and 0.5 mm long RF electrodes.




(a) (b)

***Figure 5.30.*** *Scanning electron microscope (SEM) photograph of the fabricated gap capacitors with ITO bias electrodes: (a) Short ABE capacitor (type III); (b) Long ABE capacitor (type IV).*

Since the thin ITO layer is optically transparent in visible wavelengths, scanning electron microscope (SEM) pictures are taken in the gap area for a clear structural viewgraph. Figures 5.30a and 5.30b show SEM pictures of a short ABE structure (type III) and a long ABE structure (type IV), respectively. The RF gaps are 14 μm wide, the gap of the DC bias electrode is 1.5 μm wide, and the width of the DC bias electrode is 2.5 μm wide.

Figure 5.31 shows gap capacitors with LSCO as a high resistivity material. Four different samples are shown: (a) a conventional wide gap capacitor (type I), (b) a conventional narrow gap capacitor (type II), (c) a long ABE capacitor (type IV), and (d) a long IBE capacitor (type V), respectively. Note that LSCO is visible using an optical

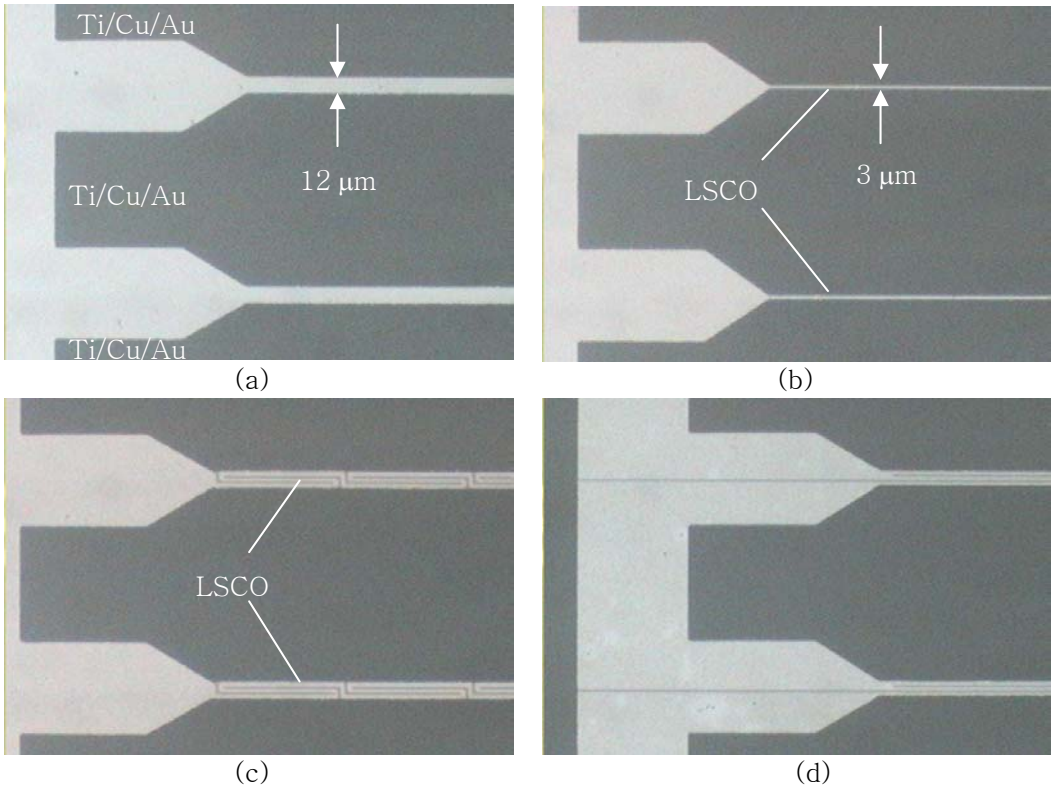



***Figure 5.31.*** *Photomicrograph of the fabricated gap capacitors with LSCO bias electrodes: (a) Wide gap capacitor (type I); (b) Narrow gap capacitor (type II); (c) Long ABE capacitor (type IV); (d) Long IBE capacitor (type V).*

microscope. The RF gap, the length of RF electrodes, the spacing of the DC bias electrode, and the width of DC bias electrode are 12 μm, 1 mm, 2 μm, and 2 μm, respectively. The length of the isolated electrodes is 1.2 mm.

#### 5.2.2.2. Experiments

##### *5.2.2.2.1. Characteristics of wide gap capacitor, long ABE capacitor, and narrow gap capacitor*

It is instructive to study the RF behavior of wide gap capacitors, narrow gap capacitors, and one of the reduced IMD capacitors (e.g., the long ABE structure) as a group. Assuming the geometries have been appropriately designed, the wide gap capacitor has the same capacitance and IMD behavior as the reduced IMD capacitor, but at greatly reduced tunability; the narrow gap capacitor has the same tunability as the reduced IMD capacitor, but at a greatly increased IMD. Hence, by comparison of the behavior of these three capacitor types, the simultaneous high tunability and low IMD of the reduced IMD architecture can be clearly seen.

The capacitance of a long ABE capacitor (type IV) fabricated using ITO and that of a conventional wide gap capacitor (type I) are compared as a function of frequency in Figure 5.32. In the low frequency region, the capacitance of the long ABE structure is attributed to the sum of the capacitance from RF electrodes ($C_{RF}$) and that from the high resistivity bias electrodes ($C_{DC}$) (Figure 4.1c). As the frequency increases, the impedance of the RF branch due to $C_{RF}$ ($=1/\omega C_{RF}$) becomes smaller while the impedance of the

highly resistive bias structure is not changing much due to its smaller frequency dependence ($R_{DC}$). In the frequency range above 10 MHz, the overall impedance of the long ABE capacitor (type IV) is dominated by the RF path, resulting in its convergence to that of the conventional no-bias structure. This result demonstrates that the highly resistive bias line is not functioning as a capacitive component in the high frequency regime. Meanwhile, the capacitance of the conventional wide gap capacitor is not dependent on the frequency, as expected.

A circuit simulation is carried out using SPICE and Microwave Office with the simplified circuit in Figure 4.1c inset to extract lumped parameter values. The simulation result of capacitance is also plotted in Figure 5.32 with solid line and dashed line for the

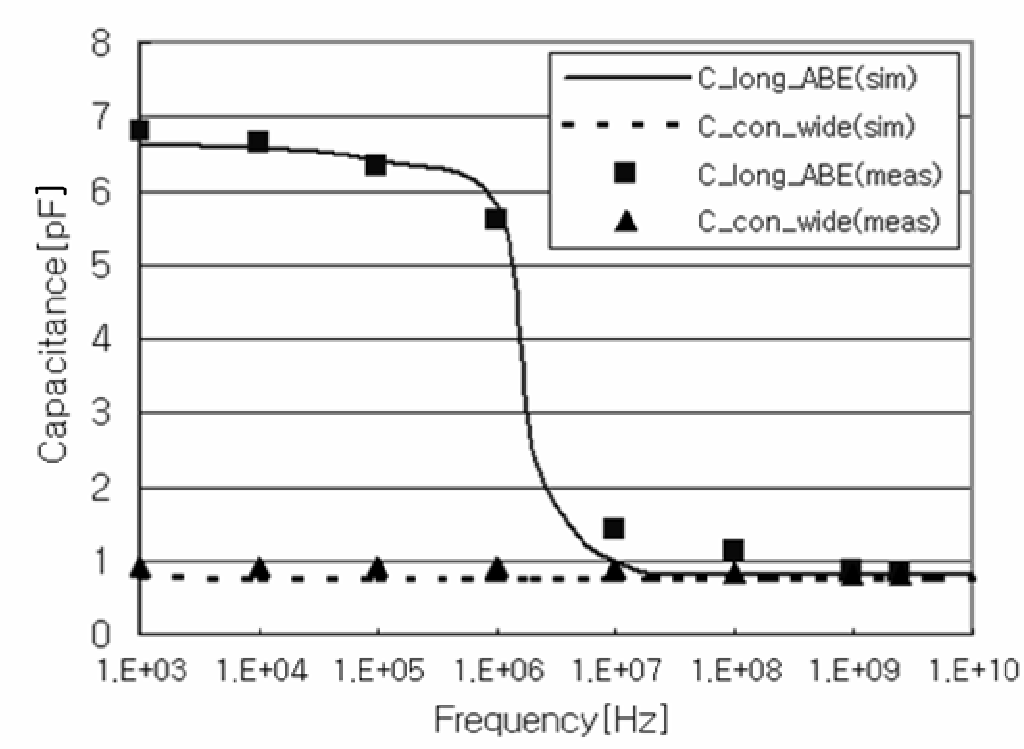


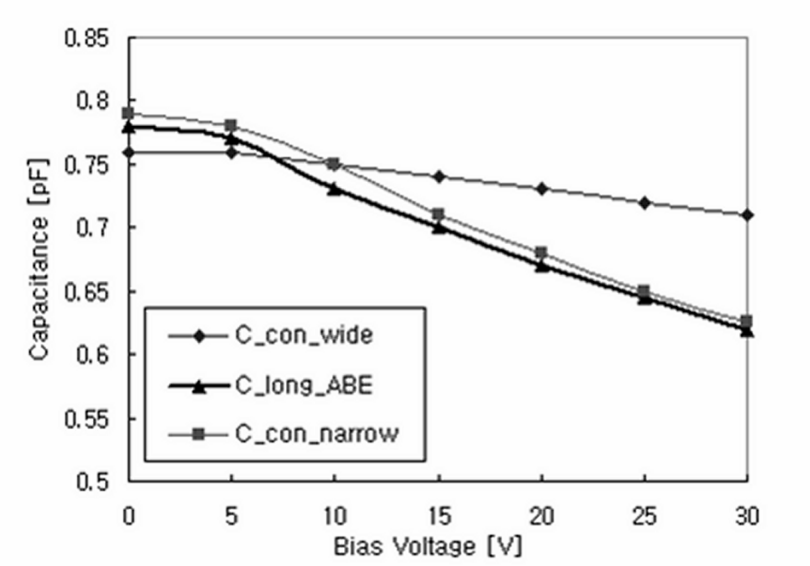

***Figure 5.32.*** *Frequency response of the capacitance for a long ABE capacitor (type IV) and a conventional no-bias structure (type I). In the legend, long_ABE and con_wide represent a long ABE capacitor (type IV) and a conventional wide gap capacitor (type I), respectively.*

long ABE capacitor (type IV) and the conventional no-bias capacitor (type I), respectively. The extracted lumped parameters used for the simulation are summarized in Table 5-2.

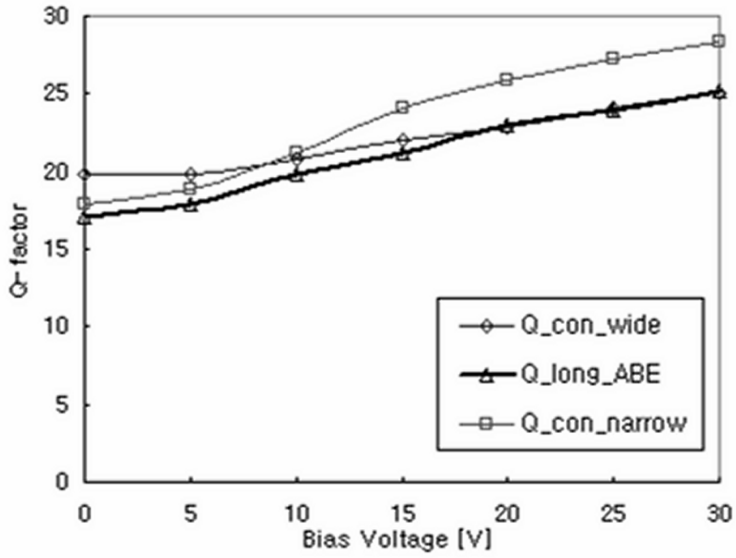
**Table 5-2.** Lumped parameters for a long attached-bias-electrode (ABE) capacitor (type IV) and a conventional gap capacitor (type I)

| | $C_{DC}$ | $R_{DC}$ | $C_{RF}$ | $R_{RF}$ |
|---|---|---|---|---|
| Long ABE capacitor (type IV) | 6.8pF | $10^5\Omega$ | 0.80pF | 5Ω |
| Wide gap capacitor (type I) | 0 | ∞ | 0.75pF | 5Ω |

The measured capacitance and quality factor for three structures (type I, type II, and type IV) as a function of the DC bias voltage at 2.5 GHz are shown in Figure 5.33. Approximate tunability ($C_{max}/C_{min}$) of 1.27 at 30V was obtained both for the narrow gap capacitor (type II) and the ABE capacitor (type IV), while a tunability of only 1.08 was obtained for the wide gap capacitor. Quality factors for all three structures were over 16 at zero bias voltage. Note that the quality factor of the proposed bias-structure (type IV) was not materially degraded due to the highly resistive bias lines, as expected.




(a)




(b)

***Figure 5.33.*** *Comparison of a conventional wide gap capacitor (type I), a long ABE capacitor (type IV), and a conventional narrow gap capacitor (type II) as a function of the DC bias voltage at 2.5 GHz: (a) Capacitance vs. bias voltage; (b) Q-factor vs. bias voltage. In the legend, con_wide, long_ABE, and con_narrow represent a conventional wide gap capacitor (type I),long ABE capacitor (type IV), and conventional narrow gap capacitor (type II), respectively. ITO is used for highly resistive DC bias electrodes.*

#### *5.2.2.2.2. Short ABE capacitor vs. long ABE capacitor*

The capacitance of a conventional gap capacitor (type I), a short ABE capacitor (type III), and a long ABE capacitor (type IV) have been measured at 100 kHz and 2.5 GHz with zero bias and 30 V to determine and compare the frequency response and tunability of these structures. The measurement data are summarized in Table 5-3. While the conventional gap capacitor (type I) shows little frequency dependence of capacitance, type III and type IV show a large capacitance transition with frequency in the same fashion as seen in Figure 5.32. However, the tunability of the short ABE capacitor (type III) at 2.5 GHz is the lowest of the three structures, which implies the DC field perpendicular to that of the RF signal is not contributing to permittivity change in the direction of the RF signal. Therefore, the short ABE (type III) structure is not suitable for reduced IMD, high tunability capacitors.

**Table 5-3.** Tunability comparison of a conventional gap capacitor (type I), a short attached-bias-electrode (ABE) capacitor (type III), and a long attached-bias-electrode (ABE) capacitor (type IV) at 100 KHz and 2.5GHz

| | | Capacitance [pF] | | | | | |
|---|---|---|---|---|---|---|---|
| | | Wide gap capacitor (type I) | | Short ABE capacitor (type III) | | Long ABE capacitor (type IV) | |
| | | 100 kHz | 2.5 GHz | 100 kHz | 2.5 GHz | 100 kHz | 2.5 GHz |
| Bias voltage | 0 V | 0.74 | 0.68 | 3.10 | 0.73 | 4.56 | 0.79 |
| | 30V | 0.69 | 0.64 | 1.86 | 0.69 | 2.40 | 0.60 |
| Tunability ($C_{max}/C_{min}$) | | 6.8% | 5.9% | 40.0% | 5.5% | 47.4% | 24.1% |

*5.2.2.2.3. Long ABE capacitor vs. long IBE capacitor*

All of the previously-discussed capacitor architectures have two bias points at signal pad S and ground pad G. The long isolated-bias-electrode (IBE) capacitor (type V) has two additional bias pads, V1 and V2. The introduction of these independent bias pads offers additional flexibility in both tuning as well as operation of the device in other applications. To assess these long IBE (type V) devices, their capacitance as a function of various bias schemes has been measured and compared with the previously-discussed type I, II, and IV devices. All of the devices characterized in this section used LSCO as the highly resistive material (Figure 5.31). The measured capacitance, tunability at 30 V, and Q-factor are summarized in Table 5-4.

The capacitance and tunability of each architecture is slightly higher, and the Q-factors slightly lower, than that of their ITO-based counterparts shown in Figures 5.29 and 5.33. However, it is not clear whether this effect is intrinsic to the LSCO versus ITO, or whether it is due to stoichiometric BST variations between each sample. In general, capacitance and tunability can be traded off against Q-factor by varying the stoichiometry of the BST film. Three different bias cases are applied to the long IBE (type V) capacitor. From the point of view of the tuning voltage, both the signal and ground pads were at or near ground since the excitation level of the RF source was low. The first case has 30 V applied to V1, with V2 held at ground. The second case has 30 V applied to V1 and –30 V applied to V2. The third case has 30 V applied to both V1 and V2. The second case shows the highest tunability (1:1.4) at 30 V, which is as high as that of the long ABE capacitor (type IV) at 30 V.

**Table 5-4.** Tunability comparison according to bias schemes

| | S[V] | G[V] | V1[V] | V2[V] | $C_0$[pF] | $C_{30}$[pF] | $T_{30}$ ($C_{max}/C_{min}$) | Q |
|---|---|---|---|---|---|---|---|---|
| Type I | 30 | 0 | | | 1.0 | 0.9 | 1.11 | 11~13 |
| Type II | 30 | 0 | | | 1.28 | 0.78 | 1.64 | 9~14 |
| Type IV | 30 | 0 | | | 1.12 | 0.78 | 1.44 | 8~11 |
| Type V | 0 | 0 | 30 | 0 | 1.28 | 0.96 | 1.33 | 7~8 |
| | 0 | 0 | 30 | -30 | 1.28 | 0.89 | 1.44 | 7~8 |
| | 0 | 0 | 30 | 30 | 1.28 | 0.97 | 1.32 | 7~9 |

*5.2.2.2.4. IMD Test*

In order to unambiguously demonstrate that the capacitor architectures discussed above result in high tunability while simultaneously achieving low IMD, two-tone IMD tests have been performed for the long ABE capacitor (type IV) and the narrow gap capacitor with 4 μm gap (type II used for the IMD reference) in Figure 5.29. The equal-power input signals are separated by 50 kHz ($f_{RF1}$ = 1.9 GHz, $f_{RF2}$ = 1.90005 GHz). A cancellation setup was used in order to keep the noise-floor of RF signal at a low level, making it possible to measure third-order intermodulation distortion power (IM3) over a wide range. Figure 5.34 shows the fundamental output power and IM3 of the reference structure (type II) and the reduced IMD capacitor (type IV) as input power varies. At low input powers (below 2 dBm), the IM3 of both capacitors are close to each other, and the difference of IM3 of the two capacitors increases with increased input power due to the noise-floor of the signal. Beyond input power of 10 dBm, the difference of IM3 is

approximately 12 dB. The input third-order intermodulation intercept point ($IIP_3$) is plotted against the input power as shown in Figure 5.35. $IIP_3$ is calculated by measuring both fundamental and IM3, and applying the following formula:

$$IIP_3 = OIP_3 - Loss = (P_{1out} + IM_3 \div 2) - Loss \qquad (5.10)$$

Approximately 6 dB improvement of $IIP_3$ was obtained beyond the input power of 10 dBm. The high frequency measurements at 2.5GHz and two-tone test results at 1.9GHz are summarized in Table 5-5. Compared with the reference structure (type II), the same tunability and 6 dB $IIP_3$ improvement using the reduced IMD capacitor (type IV or type V) can be achieved.

**Table 5-5.** Summary of high frequency measurement at 2.5GHz and two-tone test at 1.9GHz for IIP3

| | Wide gap capacitor | | **Long ABE** | | Narrow gap capacitor | |
|---|---|---|---|---|---|---|
| Capacitance [pF] | 0V | 30V | **0V** | **30V** | 0V | 30V |
| | 0.76 | 0.71 | **0.78** | **0.62** | 0.78 | 0.62 |
| Q-factor | 19.8 | 25.0 | **17.1** | **25.0** | 18.0 | 28.3 |
| Tunability ($C_{max}/C_{min}$) | 1.08 | | **1.27** | | 1.27 | |
| IIP3 | 58dBm | | **58dBm** | | 52dBm | |

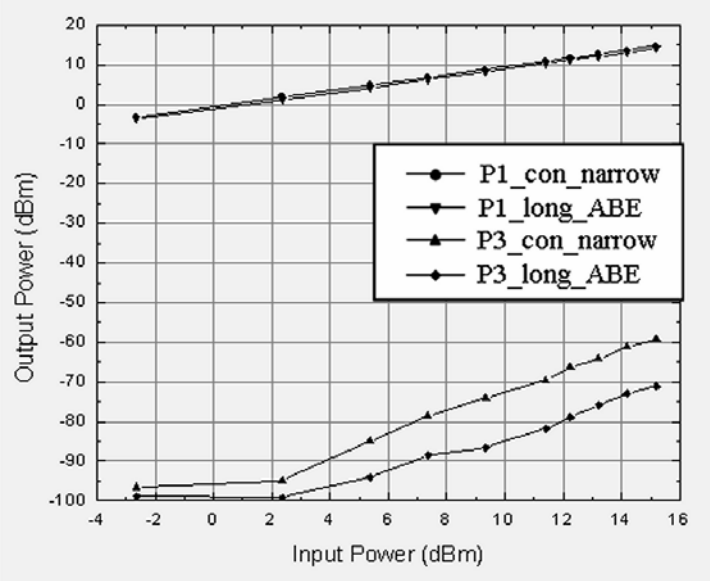



***Figure 5.34.*** *Fundamental ($P_1$) and third order intermodulation power ($P_3$) as a function of input power. In the legend, con_narrow and long_ABE represent a conventional narrow gap capacitor (type II) and a long ABE capacitor (type IV), respectively.*

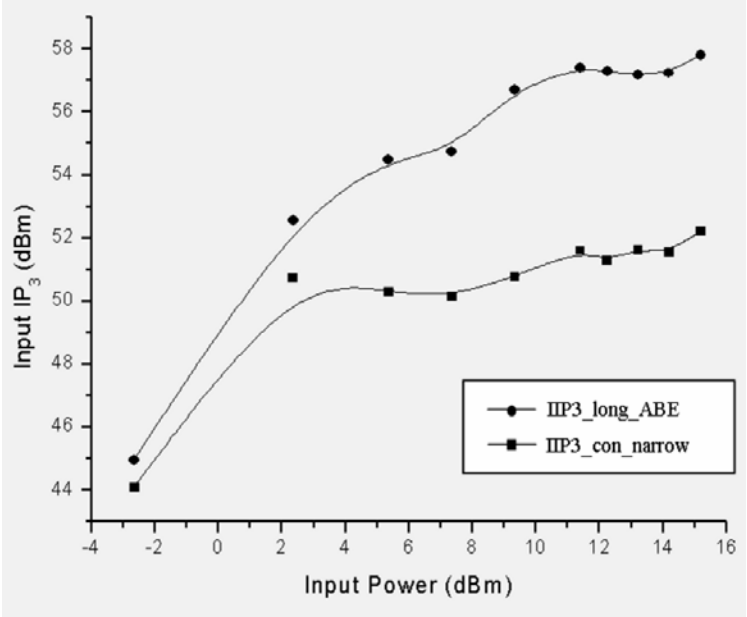



***Figure 5.35.*** *Input $IP_3$ versus input power. In the legend, long_ABE and con_narrow represents a long ABE capacitor (type IV) and a conventional narrow gap capacitor (type II), respectively.*

#### 5.2.2.3. Summary and Discussion

Low IMD tunable capacitor architectures with high resistivity DC bias structures within the RF gap were designed, fabricated, and tested. Five gap capacitor architectures (two conventional gap capacitors; type I and type II, and three bias-electrode capacitors with high resistivity DC bias structure within an RF gap; type III, type IV, and type V) were characterized in detail. Thin film oxide conductors (3~10 nm thick), such as indium tin oxide (ITO), and lanthanum strontium cobalt oxide (LSCO) are used for high resistive bias electrodes with the sheet resistance of $2\sim3\times10^4$ Ω/sq. Long attached-bias-electrode capacitor (long ABE capacitor, type IV) and long isolated-bias-electrode capacitor (long IBE capacitor, type V) are suitable architectures for low IMD tunable capacitors. The long IBE capacitor (type V) has more degrees of freedom in biasing compared with the attached-bias-electrode capacitor. The long ABE capacitor (type IV) and the long IBE capacitors (type V) showed similar overall tunability ($C_{max}/C_{min}$) of 1.4 at 30V . The performance of the reduced IMD capacitors showed 6 dB of improvement in IMD performance when compared with the equivalent conventional gap capacitor design, where both structures showed tunability ($C_{max}/C_{min}$) of 1.27 at 30 V. From frequency response and impedance measurements, it was also concluded that the DC bias structure did not significantly degrade the Q of the capacitor.

### 5.2.3. Reduced IMD Tunable Ferroelectric Capacitor : Part II

An architecture and proof of concept to reduce intermodulation distortion has been discussed in the previous section and references [93, 94], in which approximately 6dB of IIP3 improvement with the proposed scheme compared to a conventional gap capacitor has been demonstrated. In this work, the device capability is extended to a wider gap device with multi-pair high resistivity electrodes to investigate further IMD improvement with various gaps. A usage of a different high resistivity electrode material, aluminum-doped zinc oxide (AZO) is introduced. The frequency dependent capacitance parameterized by the resistivity of the high resistivity electrodes is discussed as well.

#### 5.2.3.1. Fabrication

Three gap capacitors are designed to compare architectures for reduced IMD. The three geometries are shown in Figure 5.36: (a) a conventional narrow gap with both DC gap and RF gap 4 μm; (b) a single pair gap capacitor with a DC gap of 2 μm and an RF gap of 14μm; and (c) a double pair gap capacitor with a DC gap of 2 μm and an RF gap of 20 μm.

Fabrication of the capacitor employs one etch and one lift-off step. An aluminum doped zinc oxide (AZO) material is used for the high resistivity electrodes, differing from the materials utilized in the last chapter, namely indium-tin-oxide (ITO) or lanthanum-strontium-cobalt-oxide (LSCO) [94]. This change was made for manufacturing reasons as opposed to a specific device need. The AZO is grown on top of the BST layer on a

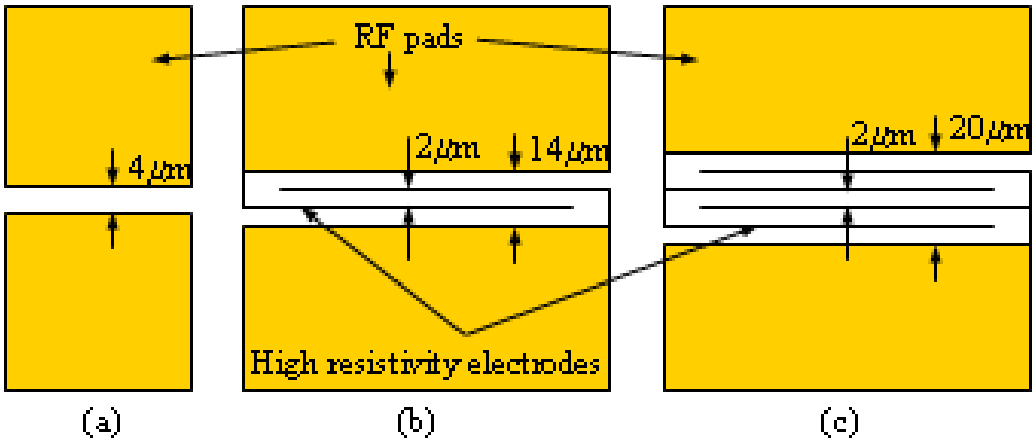
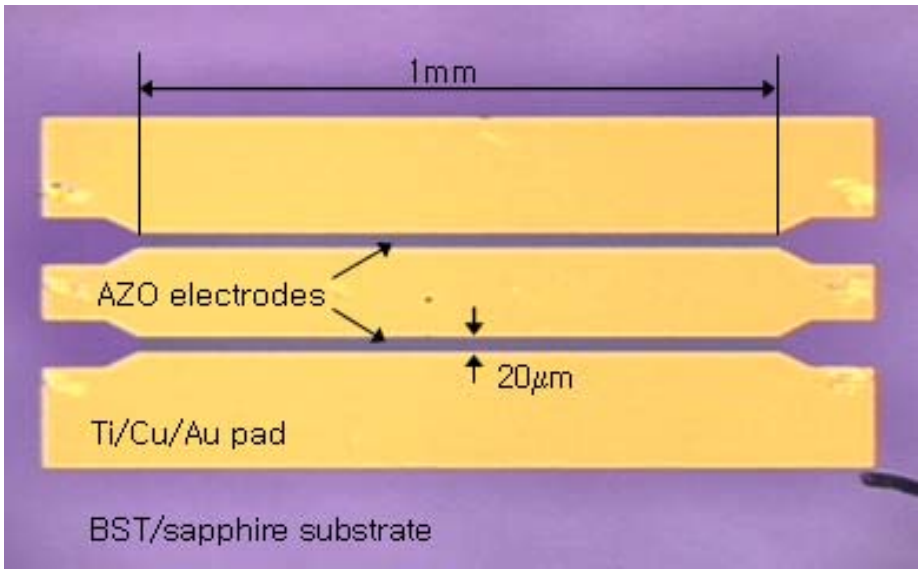



***Figure 5.36.*** *Three different capacitors: (a) Conventional narrow gap capacitor (type II), both dc bias gap and RF gap are 4 μm; (b) Single pair wide gap capacitor (type IV), dc bias gap is 2 μm and RF gap is 14 μm; (c) Double pair wider gap capacitor (type IV), dc bias gap is 2 μm and RF gap is 20 μm.*

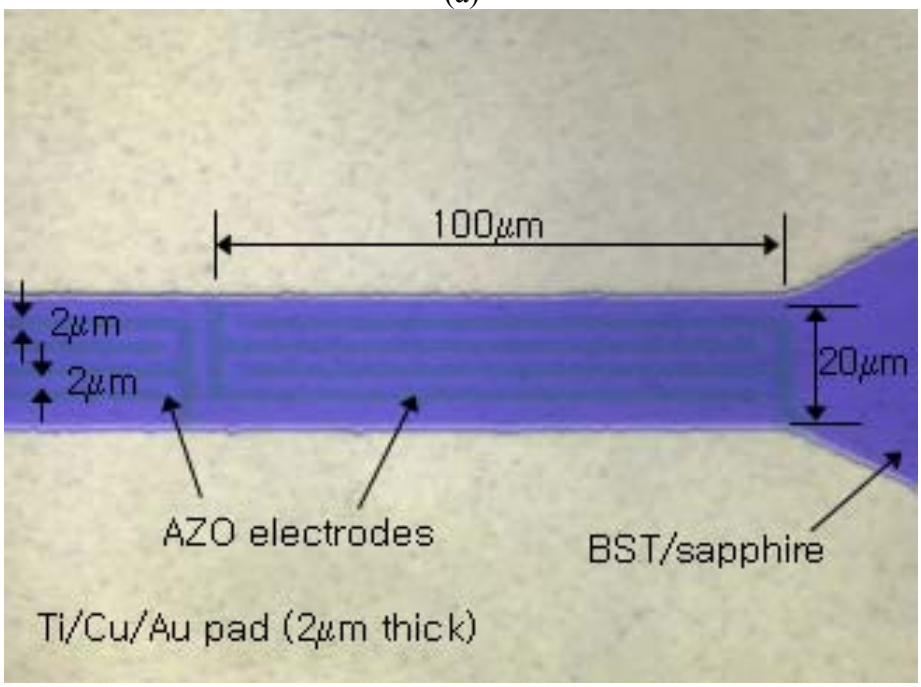
sapphire substrate by MicroCoating Technologies using a combustion chemical vapor deposition (CCVD) process [105]. AZO is patterned by etching in dilute nitric acid. The RF conductor is formed using a standard lift-off process.

To minimize the parasitic capacitance between signal and ground lines, a shunt capacitor scheme is adopted using a coplanar waveguide configuration. A fabricated device using AZO resistive electrodes is shown in Figure 5.37. Figure 5.37a shows a fabricated wide gap capacitor with double pairs of high resistivity electrodes in the gap, where the RF pad is 1 mm long and the RF gap is 20 μm wide. Figure 3.37b shows ten repeated AZO bias electrode groups with a group pitch of 100 μm, and a DC bias gap of 2 μm.

Figures 5.38a and 5.38b show SEM images of the gap areas for a single pair structure and a double pair structure, respectively.

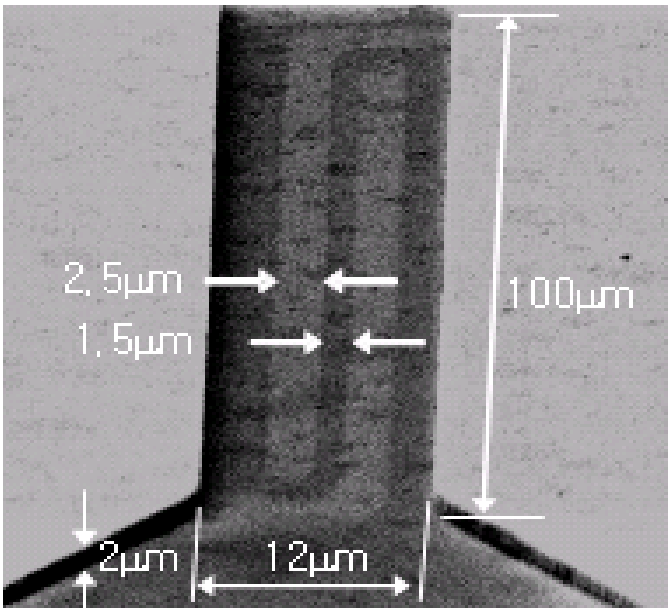



(a)

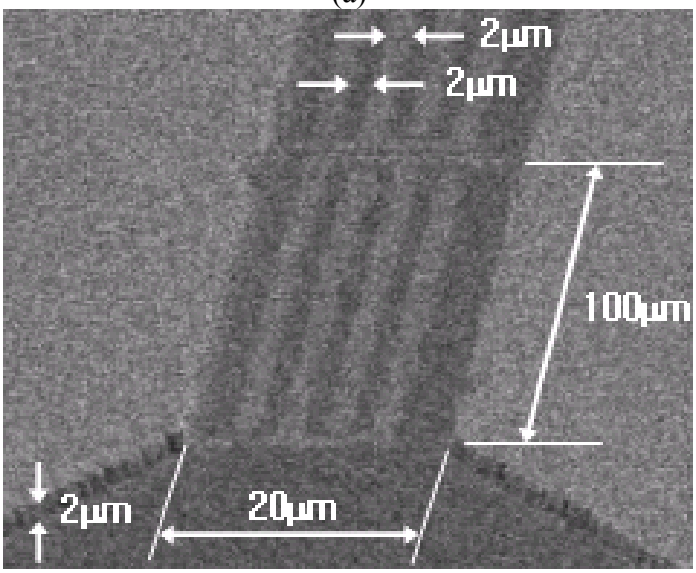



(b)

***Figure 5.37.*** *Photomicrograph of reduced intermodulation distortion (IMD) gap capacitor with high resistivity electrodes inside gaps: (a) Overall view; (b) Magnified view.*




(a)




(b)

***Figure 5.38.*** *SEM view of reduced intermodulation distortion (IMD) gap capacitor with high resistivity electrodes inside gaps: (a) Single pair structure; (b) Double pair structure.*

#### 5.2.3.2. Test and Results

S-parameter measurement is carried out in the frequency range of 300 kHz to 3 GHz using an HP8753 vector network analyzer with Cascade Microtech standard Air Coplanar G-S-G probe tips (150 μm pitch) after a standard SOLT calibration. Extracted capacitance as a function of frequency is investigated with single pair structure in Figure 5.39. Capacitors with different AZO sheet resistances (obtained by varying the aluminum doping level) show different capacitance-frequency behavior as expected. A capacitor with higher sheet resistance (32 KΩ/sq) shows a lower frequency transition compared to one with lower sheet resistance (3KΩ/sq); however the capacitance of both structures in high frequency converges to that of a conventional wide gap with no high resistivity electrodes in it.

Capacitance, tunability, and Q-factor for a conventional narrow gap structure, a single pair gap structure, and a double pair gap structure in Figure 5.36 are characterized at 2.5 GHz and summarized in Table 5-6. Capacitance of three devices is in the range of 0.54~0.62 pF with a zero bias voltage. The capacitance is decreasing with an increased applied bias voltage. Tunability ($T \equiv 100x(C_{max}-C_{min})/C_{max}$) is approximately 21 % with a DC bias of 30 V regardless of RF gap because the dc bias line pitch (which controls the DC tunability) is approximately 4 μm for all three devices. A slight degradation of Q-factor with number of pairs is observed.

A two-tone cancellation test for IMD characteristics has been performed at 1.9 GHz with the tone spacing of 100 kHz for the three devices. Fundamental (P1) and third-order intermodulation distortion power (P3) as a function of input power is measured. The

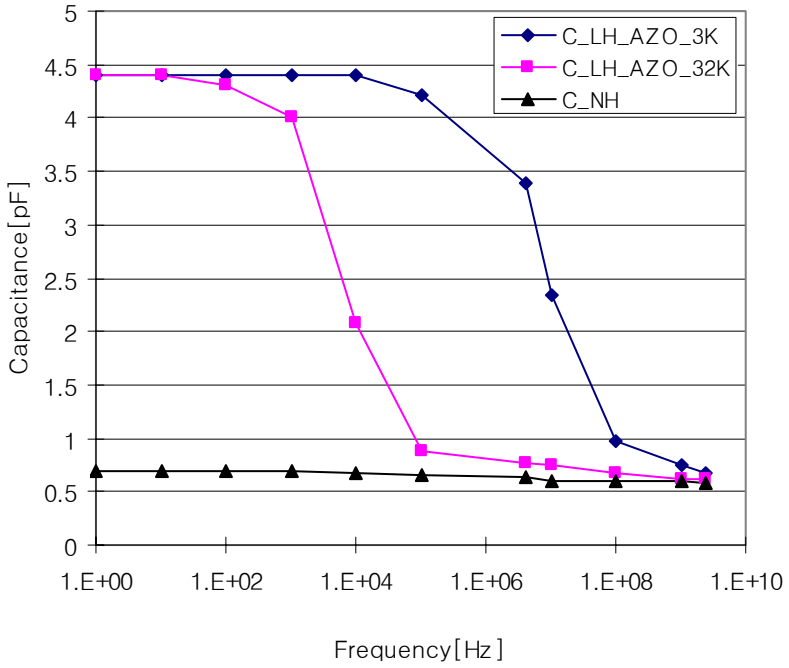



***Figure 5.39.*** *Capacitance according to operating frequency with different AZO resistivity bias lines: diamond mark represents a single pair device with sheet resistance of AZO 3 KΩ/sq and square mark with 32 KΩ/sq while triangle is for a capacitor without bias lines.*

third-order intermodulation distortion power (IM3) is plotted in Figure 5.40. It is converted to a third-order input intercept point (IIP3) according to input power. Compared to a narrow gap device with 4 μm RF gap, a single pair device with 14 μm RF gap, and the double pair device with 20μm RF gap, third-order harmonics are decreasing as the RF gap width increases. In particular, the third order harmonic output level of the double pair device is quite small due to its wide RF gap and is very close to a noise floor in the low input power. Calculated IIP3's from Figure 5.40 for all three devices are summarized in Table 5-6. The IMD improvement of a single pair structure and a double pair structure compared to a conventional narrow gap capacitor are 6 dB and 15 dB, respectively.

**Table 5-6.** Summary of high frequency measurement at 2.5 GHz and two-tone test for IIP3 at 1.9 GHz

| | Conventional Narrow Gap Capacitor | | Single Pair Structure | | Double Pair Structure | |
|---|---|---|---|---|---|---|
| Bias voltage [V] | 0 | 30 | 0 | 30 | 0 | 30 |
| Capacitance [pF] | 0.58 | 0.46 | 0.62 | 0.49 | 0.54 | 0.42 |
| Q-factor | 21 | 48 | 16 | 28 | 13 | 23 |
| Tunability [%] | 20.7 | | 20.9 | | 22.2 | |
| IIP3 [dBm] | 47 | | 53 | | 62 | |

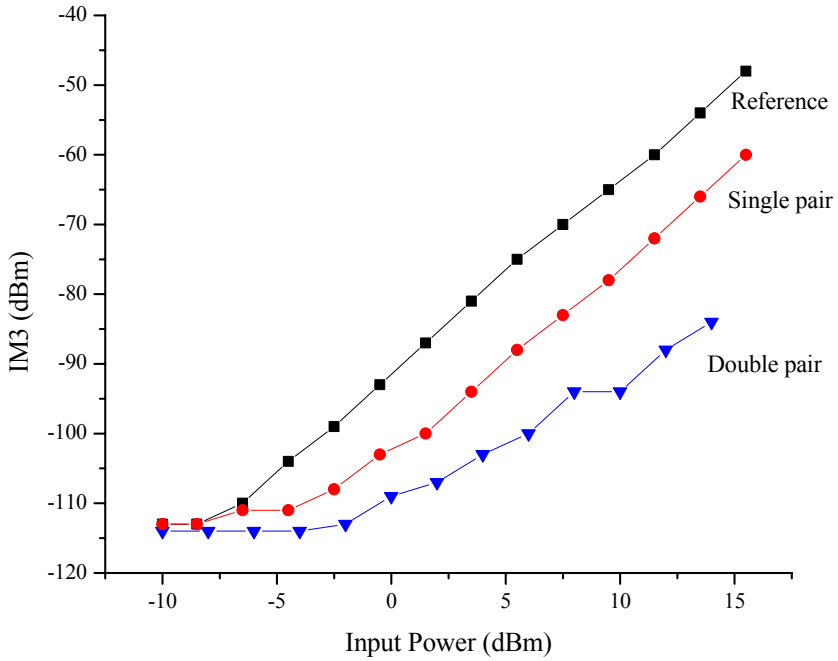



***Figure 5.40.*** *Third order intermodulation distortion power (P3) with different geometry as a function of input power.*

#### 5.2.3.3. Summary and Discussion

Intermodulation distortion (IMD) improvement has been demonstrated with three devices: a conventional narrow gap capacitor, a single pair gap capacitor, and a double pair gap capacitor. A 14 μm gap and a 20 μm gap capacitor show better IMD performance compared by a 4 μm gap capacitor by 6 dB and 15 dB, respectively, while the tunability is approximately 21 % at 30 V for all three devices with narrowly spaced multi-pair high resistivity dc electrodes in it. Aluminum doped zinc oxide (AZO) is used for a high resistivity electrode material. A capacitor with higher sheet resistance of AZO shows a capacitance transition at lower frequency.

## 5.3. RF Compact Tunable LC Module

In this section, a distributed gap capacitor is fabricated on top of a ferroelectric material in a spiral inductor shape, by which a compact tunable LC module is formed.

### 5.3.1. Design and Fabrication

A schematic view of the generic tunable LC module characterized in this work is shown in Figure 5.41. The structure consists of an extended gap capacitor, which functionally has the structure discussed in previous sections, with the additional feature

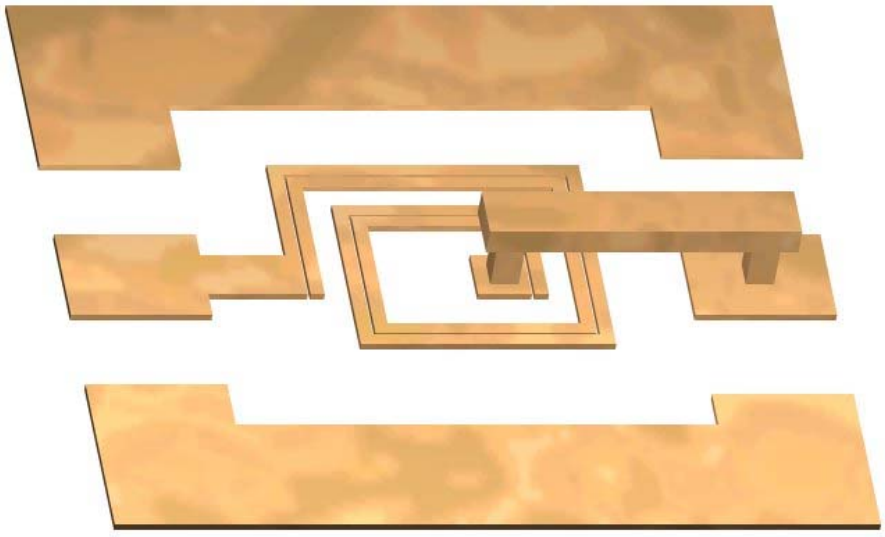


***Figure 5.41.*** *A tunable LC module schematic.*

that the extended gap capacitor is wound in the shape of an inductive coil, thereby bringing the self-resonant frequency of the structure into the RF frequency range of interest. Since the capacitor dielectric is tunable, this self-resonant frequency can be controlled by altering the voltage across the extended gap capacitor. In this way, a single filter can be formed simply by appropriate alteration of the geometry of the gap capacitor.

Three LC modules based on this generic structure have been designed. As shown in Figure 4.5b, each structure consists of a narrow gap capacitor portion with a length of $l_1$, and a non-capacitor portion with lengths of $l_2$, and $l_3$. The overall device footprint is 460 μm by 420 μm for all devices. Their dimensions are summarized in Table 5-7.

**Table 5-7.** Tunable LC module geometry

| | LC I | LC II | LC III |
|---|---|---|---|
| $l_1$ [μm] | 3440 | 2080 | 1040 |
| $l_2$ [μm] | 1700 | 3060 | 4100 |
| $l_3$ [μm] | 560 | 560 | 560 |

The fabrication process is detailed in Figure 5.42. Epitaxially grown BST on sapphire is used as a substrate (deposition is done by combustion chemical vapor deposition (CCVD) at Microcoating Technology Inc.). A gap capacitor with a gap of 1.5 μm, a width of 10 μm, and an electrode thickness of 2.5 μm and a spiral inductor portion are patterned using a lift-off process. Thick metal electrodes with a narrow gap are employed to reduce conductor loss, fabricated using a low-loss conductor fabrication technique (a). In order to form the return path of the inductor, a photoresist of 25μm thick

is patterned for vias, followed by a conformal seed layer deposition of titanium/copper with DC sputtering. The second photoresist is patterned for bridge formation (b). Copper and gold electrodeposition is performed in sequence. The photoresist layers and the seed layers are removed sequentially to complete the devices (c).

A fabricated tunable LC module is shown in Figure 5.43. The device area is 420 μm by 460 μm. The narrow gap, the electrode width, and the space between electrodes are 1.5 μm, 10 μm, and 18.5 μm, respectively.

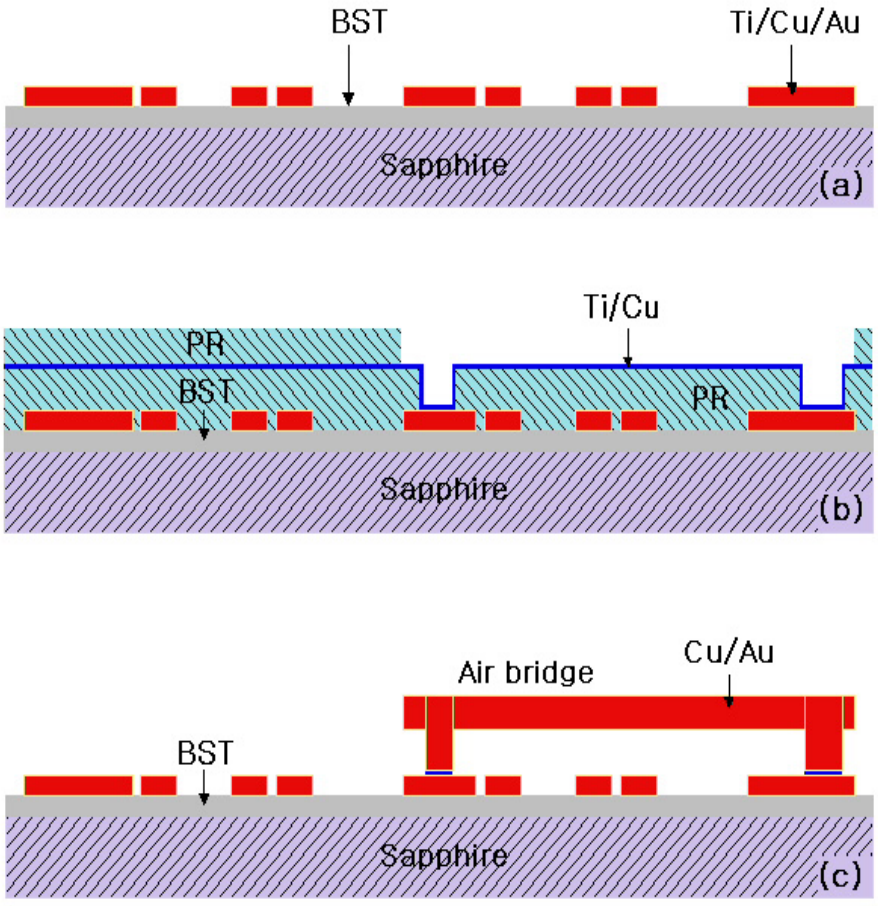
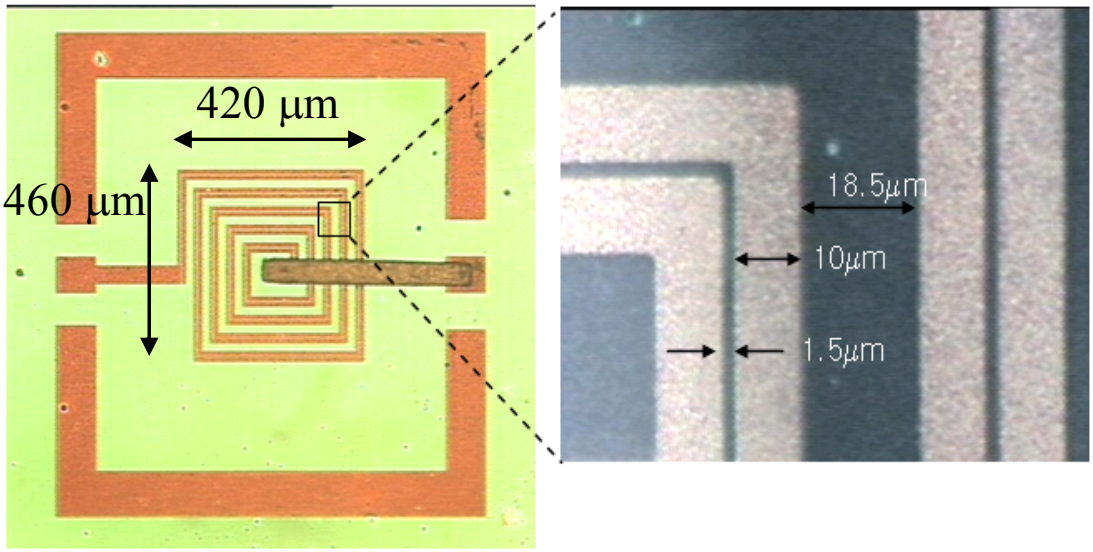



***Figure 5.42.*** *Fabrication process of a compact tunable LC module.*




(a) (b)

***Figure 5.43.*** *Tunable LC module fabricated on a BST coated sapphire substrate: (a) Overall top view; (b) Magnified view.*

### 5.3.2. Characterization

After a standard SOLT 2-port calibration using HP 8510 vector network analyzer and a probe station, s-parameters are measured with three devices. The effective capacitance is plotted in Figure 5.44. The capacitance and the resonance frequency for the LC I, LC II, and LC III are 5.74pF, 3.51pF, and 1.91pF, and 874 MHz, 1.15 GHz, and 1.65 GHz, respectively.

Capacitance as a function of coupling length is shown in Figure 5.45. Linear fitting shows capacitance per unit length of 1.7pF/mm. The lumped parameter for the equivalent circuit in Figure 4.6c is summarized in Table 5-8.

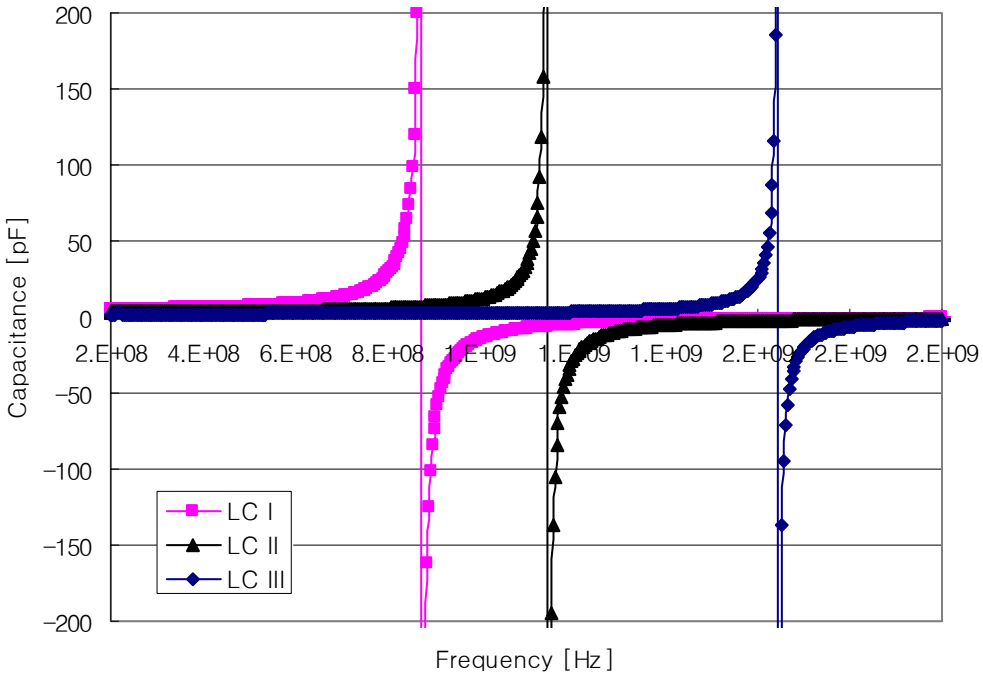



***Figure 5.44.*** *Effective capacitance extracted from s-parameter as a function of the frequency.*

**Table 5-8.** Lumped parameters of equivalent circuits for three fabricated LC modules

| | LC I | LC II | LC III |
|---|---|---|---|
| $R_{eq}$ [Ω] | 5.03 | 5.98 | 8.09 |
| $L_{eq}$ [nH] | 5.78 | 5.46 | 4.88 |
| C [pF] | 5.74 | 3.51 | 1.91 |
| $f_0$ [GHz] | 0.874 | 1.15 | 1.65 |
| Q | 6.3 | 6.6 | 6.3 |

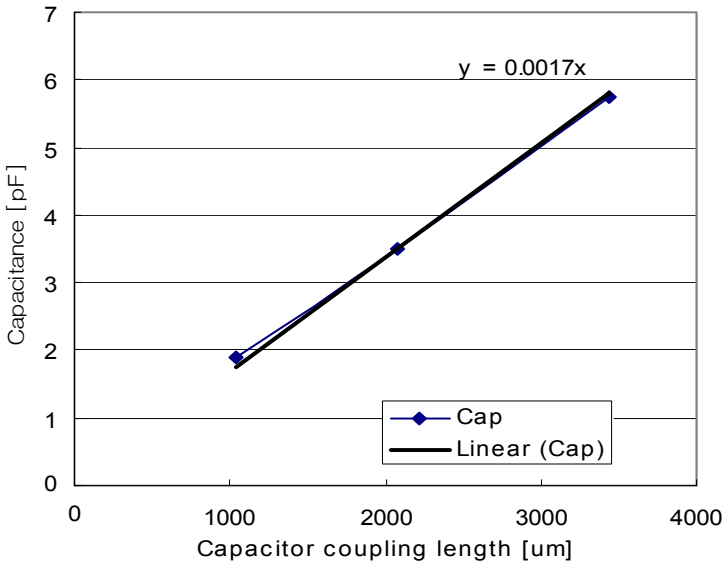



***Figure 5.45.*** *Capacitance as a function of the coupling length.*

Figure 5.46 shows capacitance and tunability as a function of DC bias voltage at 300 MHz. Tunability [%] (=100X($C_V$-$C_0$)/$C_0$) is approximately 44 % at a bias voltage of 30 V.

As capacitance decreases with DC bias voltage, the resonance frequency increases correspondingly. Figure 5.47 shows the resonance frequency change according to the DC bias voltage. The resonance frequency shows approximately linear dependence on the DC bias voltage. The frequency shift rate is approximately 1.1 %/V for all three devices. Tunability and frequency shift at 30 V is summarized in Table 5-9.

**Table 5-9.** Tunability and resonance frequency change at 30 V

| | LC I | LC II | LC III |
|---|---|---|---|
| Tunability [%] | 44.3 | 41.6 | 33.5 |
| ∫$f_0$ [MHz]<br>(%) | 290<br>(33.2) | 383<br>(33.4) | 525<br>(31.9) |

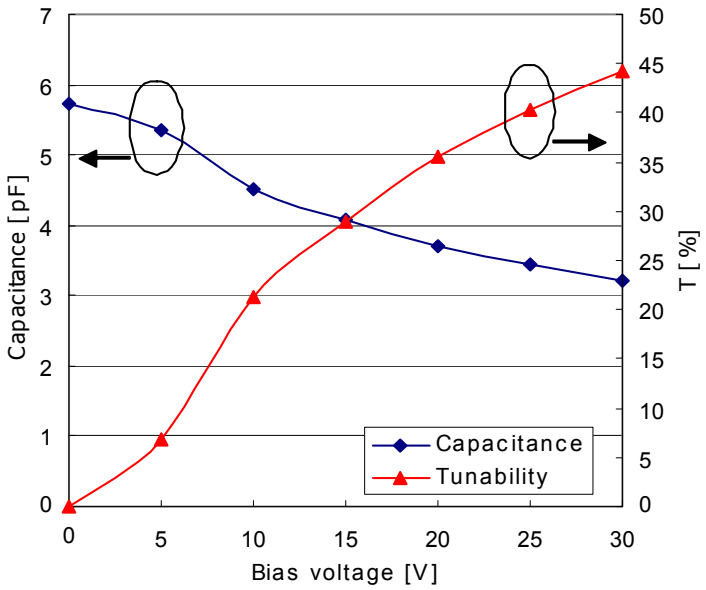



***Figure 5.46.*** *Capacitance and tunability as a function of bias voltage.*

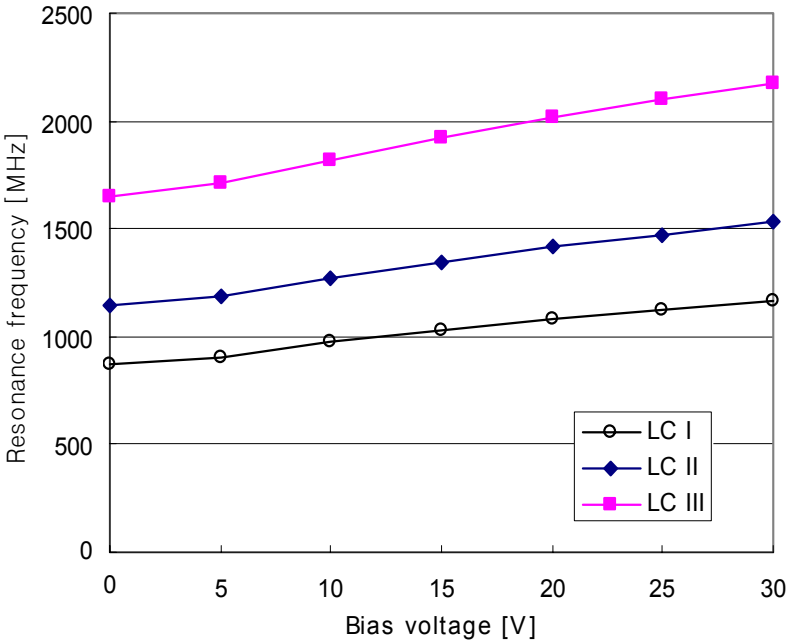



***Figure 5.47.*** *Resonance frequency as a function of bias voltage.*

### 5.3.3. Summary and Discussion

An area-effective architecture to create a tunable LC module from tunable gap capacitors is proposed by using a distributed ferroelectric gap capacitor patterned in an inductive shape. Three LC modules are designed, fabricated, and tested based on this architecture. The gap capacitor and inductor path are simultaneously fabricated. The device area is 460μm by 420μm. The resonance frequency is controllable by changing the capacitor coupling length with the overall footprint fixed. The linear resonance frequency shift is observed with DC bias up to 30 V. Frequency shift rate is approximately 1.1 %/V for all three devices.

## 5.4. W-band monopole antennas

Millimeter-wave (MMW) devices are highly valued for their ability to provide very-broad-bandwidth wireless communication in both space and terrestrial applications. Examples include satellite, radar, mobile collision detection, imaging, and indoor local communications [4, 5]. One of the key components for a wireless millimeter wave system is its radiating structure, i.e., its antenna. Currently, planar MMW antennas such as microstrip antennas or printed-circuit patch antennas are widely used due to their ease of manufacture, low cost, simple fabrication, and relative ease of integration with monolithic systems. However, patch antennas can suffer from relatively narrow bandwidth, substrate dielectric loss, mutual coupling with their substrate, and surface wave perturbation issues [**7**]. Although wire antennas (e.g., dipole or monopole antennas) or cavity antennas can be considered as alternatives to printed-circuit patch antennas because of their broad bandwidth, low loss, and reduced dependence on substrate, fabrication difficulty has prevented them from being efficiently implemented in a cost effective, integrated fashion.

Now we are at a unique intersection point in time in which increases in operation frequencies of RF systems have pushed characteristic sizes of RF subelements small enough, and advances in fabrication technologies have pushed achievable thicknesses of surface micromachined components large enough, that an intersection has been achieved. Surface micromachined radiators in the 30 - 300 GHz range (millimeter wave range) are now feasible not only in the horizontal dimension but also in the vertical dimension, offering the potential to create radiating structures with better performance than, e.g.,

conventional printed-circuit patch antennas. Surface micromachining of these devices also offers the advantages of substrate independence as well as ease of integration with chips or substrates. The purpose of this work is to illustrate the capability of surface micromachining to create radiating structures for MMW applications.

An electromagnetic wave propagating through a good conductor attenuates very quickly in the depth direction of the conductor; the resultant electric current flows through the outermost portion of the conductor. Therefore, thin (micron-scale) metal layers deposited on three-dimensional (3-D) epoxy backbones should be sufficient to create RF components whose electrical characteristics are equivalent to those of their solid metal counterparts. This concept has been demonstrated previous section for non-radiating passive elements: RF MEMS based on epoxy-core conductors in Chapter 5.1.2 [105], in which fabrication of a high-aspect-ratio RF inductor with height on the order of 1 mm has been successfully demonstrated. The three-dimensionally (3-D) complex structures achievable using mm-thickness, photostructurable resists [74, 75, 88, 89, 91] can now also create attractive geometries for high frequency radiators.

In this section, to illustrate this approach, a W-band (75 GHz ~ 110 GHz), coplanar-waveguide (CPW)-fed, quarter-wavelength monopole antenna is designed, fabricated, and characterized. This antenna has several unique properties. First, it is fed using a coplanar waveguide, which provides easy connectivity to other components and ease of fabrication compared to a via-through-substrate approach. Second, the epoxy core technique is used to provide a simple and efficient methodology for the transition from 2-D CPW structure to 3-D monopole. Third, since the fabricated monopole antenna is

achieved by a low-temperature, foundry-compatible process, fully-integrated millimeter wave systems are feasible.

### 5.4.1 Half Wave Dipole and Quarter Wave Monopole

A monopole antenna is considered as a dipole antenna that has been divided in half at its center feed point. An analysis of a quarter-wavelength monopole antenna can be deduced from that of a half-wavelength dipole antenna. A half wave dipole antenna is a resonant antenna having a standing wave over the length and zero input reactance at resonance, thus eliminating the need for tuning to achieve a conjugate impedance match. A dipole oriented along the z-axis is depicted in Figure 5.48a. It is fed at the center and the currents of each wire are equal in magnitude and opposite in direction. The current distribution along the antenna is assumed to be sinusoidal and current-distribution

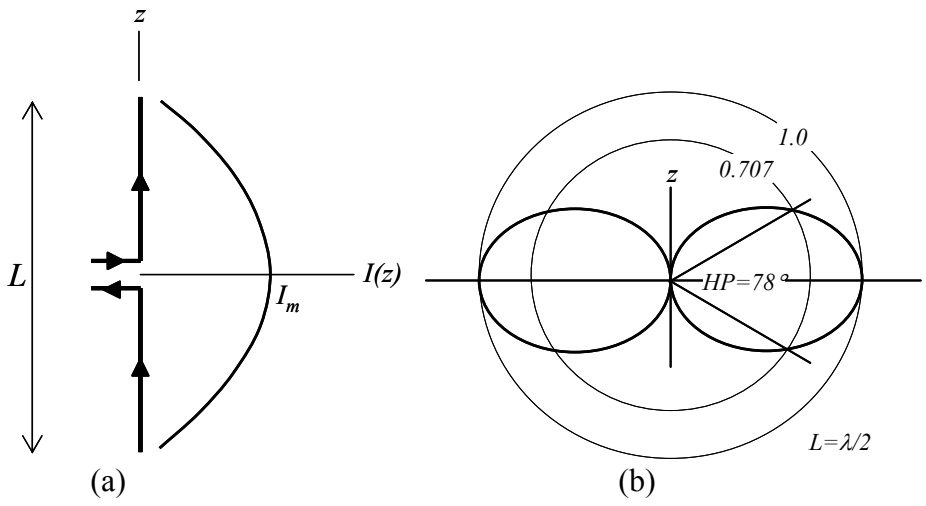



***Figure 5.48.*** *A center-fed dipole antenna: (a) Schematic and current distribution when L=λ/2; (b) Radiation pattern when L=λ/2.*

measurements indicate that it is a good assumption as long as the antenna is thin and based on ideal wire made of good conductors [106]. It can be written as Equation 5.11:

$$I(z) = I_m \sin[\beta(\frac{L}{2} - |z|)], \qquad |z| < \frac{L}{2} \qquad (5.11)$$

where $I_m$ is the peak current and $\beta$ is the wave constant ($=2\pi/\lambda$, $\beta^2=\omega^2\mu\varepsilon$).

The far-field electric and magnetic field of a dipole antenna is determined by integrating the fields for an infinitesimal dipole of length *dz* at a distance *r* from the antenna:

$$E_\theta = j\eta I_m \frac{e^{-j\beta r}}{2\pi r} \frac{\cos[(\beta L/2)\cos\theta] - \cos(\beta L/2)}{\sin\theta} \qquad (5.12)$$

$$H_\phi = jI_m \frac{e^{-j\beta r}}{2\pi r} \frac{\cos[(\beta L/2)\cos\theta] - \cos(\beta L/2)}{\sin\theta} \qquad (5.13)$$

where $\eta$ ($=(\mu/\varepsilon)^{0.5}$) is the intrinsic impedance of the medium which is $120\pi$ in air.

The θ-variation of this function determines the far-field pattern. For L=λ/2, the normalized far-field pattern *F(θ)* is written in Equation 5.14 and depicted in Figure 5.48b.

$$F(\theta) \equiv \frac{E_\theta}{E_{\theta,\max}} = \frac{\cos[(\pi/2)\cos\theta]}{\sin\theta} \qquad (5.14)$$

The half-power beamwidth (HP) is shown as 78° in Figure 5.48b.

The radiation power $P$ is calculated by integrating the Poynting vector over the sphere surrounding the dipole antenna. It is expressed in simple terms for the half wave dipole in air as Equation 5.15:

$$P = 36.5 I_m{}^2 \qquad (L = \lambda/2) \qquad (5.15)$$

Radiation resistance $R_r$ is then calculated from Equation 5.16.

$$R_r = \frac{2P}{I_m{}^2} = 73\Omega \qquad (L = \lambda/2) \qquad (5.16)$$

In practice, the input resistance is calculated using simple empirical formulas for different pole length as in Table 5-10 [107].

**Table 5-10.** Simple formula for the input resistance of dipoles and monopoles

| Length L | Input resistance of dipole [Ω] | Input resistance of monopole [Ω] |
|---|---|---|
| $0 < L < \lambda/4$ | $20\ (\pi L/\lambda)^2$ | $10\ (\pi L/\lambda)^2$ |
| $\lambda/4 < L < \lambda/2$ | $24.7\ (\pi L/\lambda)^{2.4}$ | $12.35\ (\pi L/\lambda)^{2.4}$ |
| $\lambda/2 < L < 0.637\lambda$ | $11.14\ (\pi L/\lambda)^{4.17}$ | $5.57\ (\pi L/\lambda)^{4.17}$ |

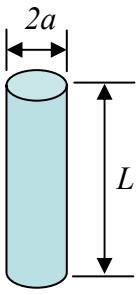
Input impedance $Z_A$ of an ideal half wave dipole is expected to have only resistance term when $L=\lambda/2$, however in the real structure, the impedance has a reactance term attributable to its wire thickness. For example, the calculated input impedance for very thin dipole (not zero) using the induced emf method [106] shows a reactance term as well as resistance:

$$Z_A = 73 + j42.5\Omega \qquad (L = \lambda/2) \qquad (5.17)$$

In fact, the dipole antenna has resonance at a slightly shorter dipole length than λ/2, where the reactance term is zero. As the wire thickness increases, the inductance contribution from the thick wire is more significant, thus the dipole should be further shortened to accomplish resonance.

Table 5-11 shows approximate wire length for resonance with various wire diameter *2a* and length *L* [106].

**Table 5-11.** Wire length required to achieve resonance with a half wave dipole or a quart wave monopole in the case of a cylindrical wire with a diameter of *2a* and a length of *L*

| Length to diameter ratio (*L/2a*) | Shortening required [%] | Resonant length | | thickness class | Geometry |
|---|---|---|---|---|---|
| | | Dipole (L) | Monopole(L/2) | | |
| 5000 | 2 | 0.49λ | 0.245λ | Very thin |   |
| 500 | 4 | 0.48λ | 0.24λ | Thin | |
| 50 | 5 | 0.475λ | 0.238λ | Less thick | |
| 10 | 9 | 0.455λ | 0.228λ | Thick | |

### 5.4.2 Design and Simulation

To design an integrated type monopole antenna, fabrication limitations and their associated effect on antenna frequency must be taken into account. Limitations exist for both achievable aspect ratio (height to diameter ratio, *h/2a* in Figure 5.49) as well as achievable absolute monopole height corresponding to the frequency range of interest.

The height of a quarter-wavelength monopole in W-band (75 GHz ~ 110 GHz) is in the range of 1 mm to 680 μm. The feasibility of tall RF conductor fabrication (up to 1mm) with aspect ratios of 10 to 15 was demonstrated in a previous work [105]. Since the monopole is cylindrical with a diameter of *2a* rather than an ideal wire with zero thickness. The non-ideal cylindrical monopole therefore has an inductive reactance term attributable to the nonzero width of the conductor when it is driven at the radiating resonance frequency of an ideal monopole of the same height. This reactance term results

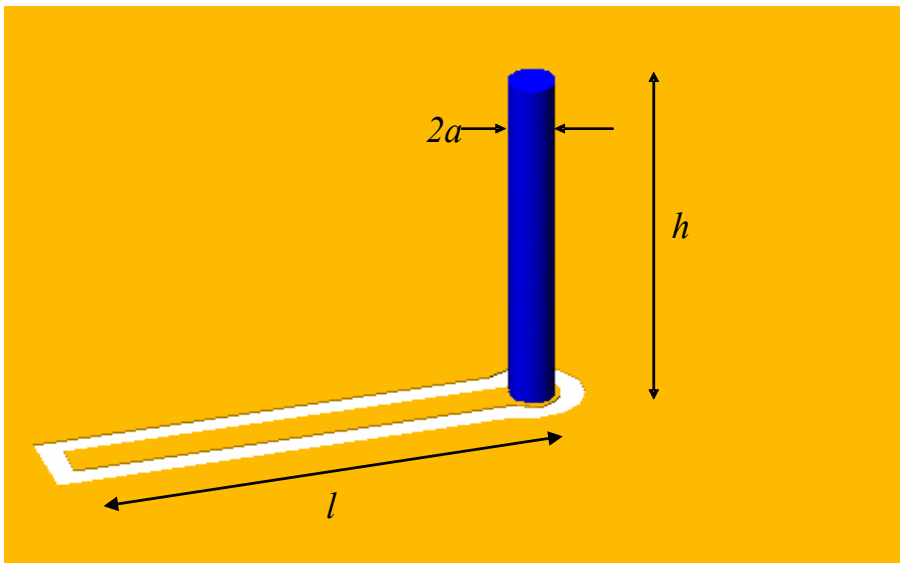



***Figure 5.49.*** *Schematic of a coplanar-waveguide fed quarter-wavelength monopole antenna.*

in the non-ideal monopole having its actual resonance at a slightly lower frequency than that of an ideal monopole. Alternatively, if a particular resonant frequency is desired, the monopole length can be reduced to achieve the ideal monopole resonant frequency. The magnitude of this height correction depends on the aspect ratio of the cylinder [106]; for example, in the case of a typical fabrication-limited aspect ratio of 10, the height $h$ of the 'quarter-wavelength' monopole is given to be $0.228\ \lambda$ from Table 5-11. The height of the quarter-wavelength monopole required for radiation resonance in W-band is plotted in Figure 5.50, where the dotted line and the solid line represent an uncompensated ideal monopole and a compensated practical monopole with an aspect ratio of 10, respectively. In addition to the height corrections discussed above, it should be noted that the thicker the cylindrical monopole (i.e., the lower the aspect ratio), the wider its bandwidth becomes, and the less sharp its band-selectivity becomes.

Although the actual radiation resistance should be calculated using methods that take into account parasitics, driving elements, and imperfect ground planes, it is instructive to consider some simplified design equations for the micromachined monopole. For a quarter-wavelength monopole antenna of aspect ratio less than infinity over an ideal ground plane, the empirical radiation resistance $R_A$ is given by Equation 5.18 from Table 5.10:

$$R_A = 12.35\ (2\pi h/\lambda)^{2.4} \qquad (5.18)$$

Using a fabrication-limited aspect ratio of 10, and a resultant height $h$ of $0.228\ \lambda$, the predicted radiation resistance is 29.3 Ω. The ohmic resistance $R_{ohmic}$ of the antenna conductor can be calculated using Equation 5.19:

$$R_{ohmic}[\Omega] = R_s \frac{h}{2\pi a} \quad , \qquad (5.19)$$

where $R_s$ is the surface resistance or sheet resistance defined as:

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}} \quad , \qquad (5.20)$$

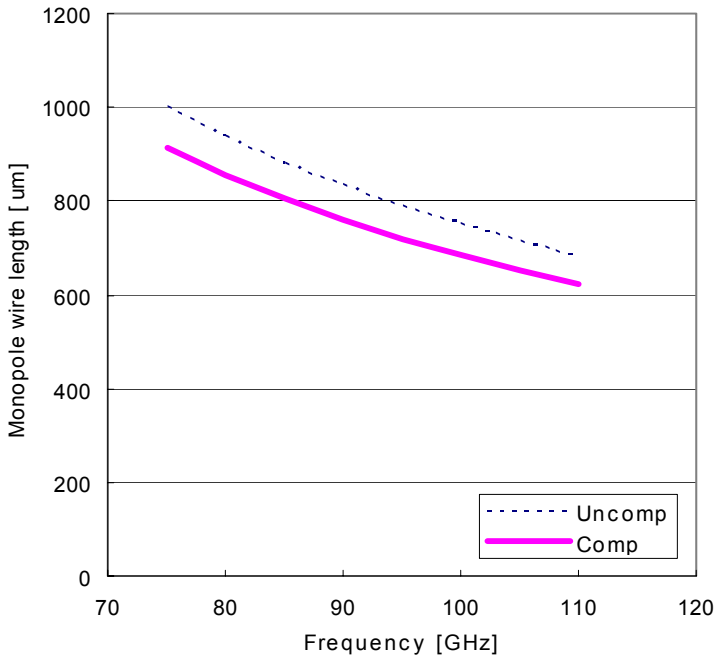
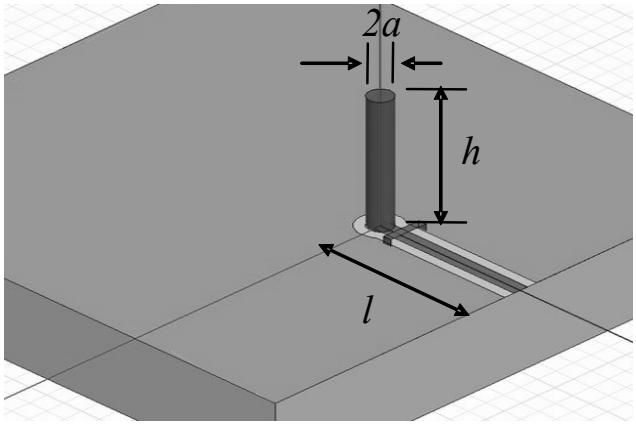



***Figure 5.50.*** *Wire length for a quarter wave monopole in W-band frequency: Uncomp and Comp represent the quarter wave length of ideal monopole and that of thick cylindrical wire, respectively. The aspect ratio of wire length to diameter is 10.*

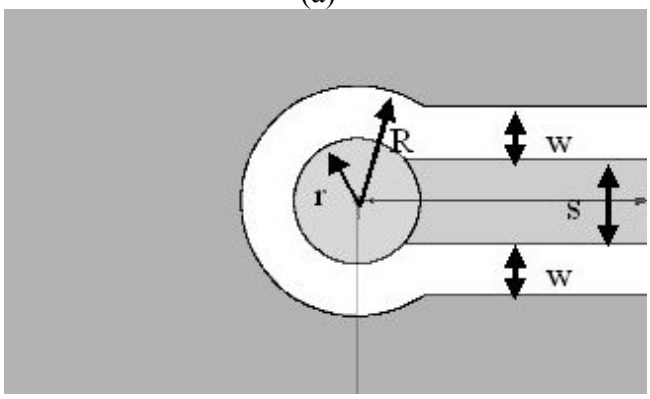
and $\omega$, $\mu$, and $\sigma$ are the radian frequency, permeability of the conductor, and conductivity of the conductor, respectively.

If the wire is made of gold ($\sigma = 4.1 \times 10^7$ S/m), the surface resistance $R_s$ at 85 GHz is calculated to be 0.092 Ω/sq. With $h$ of 800 μm and $a$ of 40 μm, $R_{ohmic}$ is 0.29 Ω. The ohmic resistance of the wire is less than 1% of the radiation resistance. Therefore, the antenna input resistance can be approximated by the antenna radiation resistance in resonance mode.

Another consideration of the monopole design is the scheme required to feed it. A




(a)




(b)

***Figure 5.51.*** *Monopole antenna fed through coplanar waveguide: (a) Overall view; (b) Top view showing geometrical parameters [108].*

monopole is usually fed against a large solid ground plane, which requires via fabrication through the substrate. Instead, here a coplanar-waveguide (CPW) feeding scheme is used as shown in Figure 5.51, resulting in a via-free and a low-cost solution for an integrated RF transceiver system.

The characteristic impedance on silicon ($\varepsilon_r$=11.7), sapphire ($\varepsilon_r$=10), and glass ($\varepsilon_r$=7.8) has been calculated as a function of the normalized center conductor width, using the LineCal functionality of the Agilent advanced design system (ADS) and is shown in Figure 5.52. The gap width *w* is fixed to 50 μm and the ground is assumed to be infinite. The calculated characteristic impedance on these substrates is between 50 Ω and 60 Ω with a central conductor width *s* of 80 μm, which is appropriate for the impedance matching to the system (its characteristic impedance is usually 50 Ω) but may not be

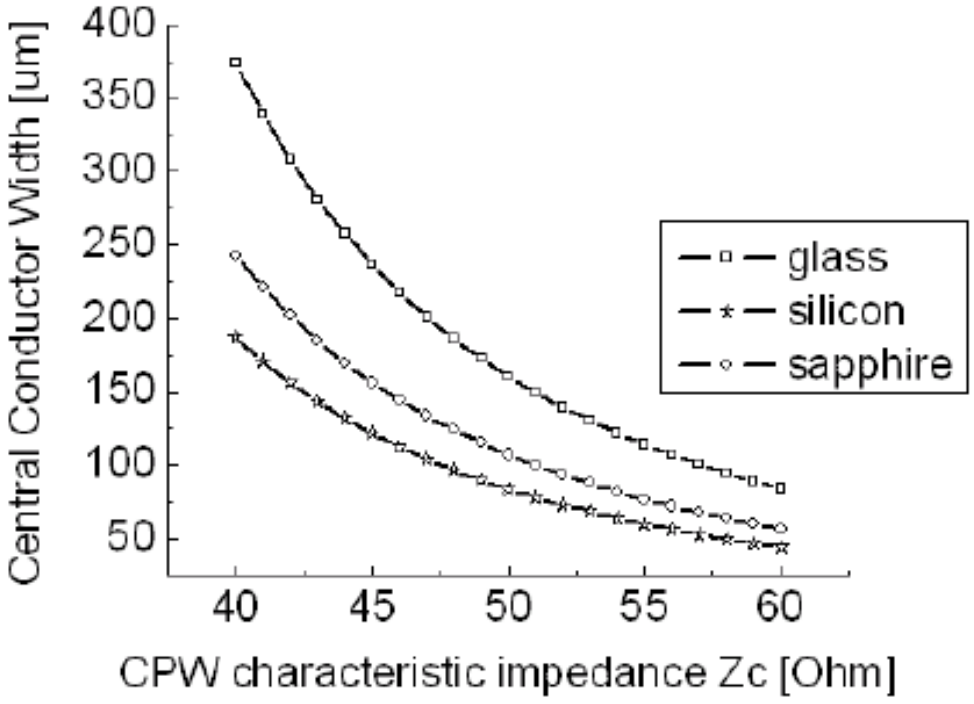



***Figure 5.52.*** *Central conductor width of CPW according to characteristic impedance Zc on different substrates (gap width is fixed to 50μm) [108].*

good for antenna input impedance matching, which could be solved by CPW geometry optimization.

For a more synthetic analysis, the monopole antenna and the feeding CPW line can be analyzed as a whole using numerical software. Input return loss and radiation pattern have been simulated using the Ansoft high frequency system simulator (HFSS) 9.0 with the parameters listed below on various substrates.

The radius of ground aperture $R$: 110 μm

The radius of bottom pad of monopole $r$: 60 μm

Gap between the signal and the ground lines $w$: 50 μm

Central conductor line width $s$: 80 μm

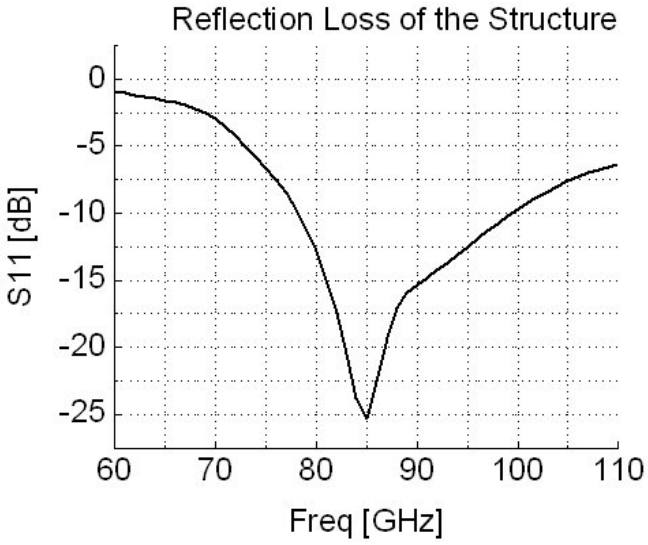
Monopole width $2a$: 80 μm

Monopole height $h$: 800 μm

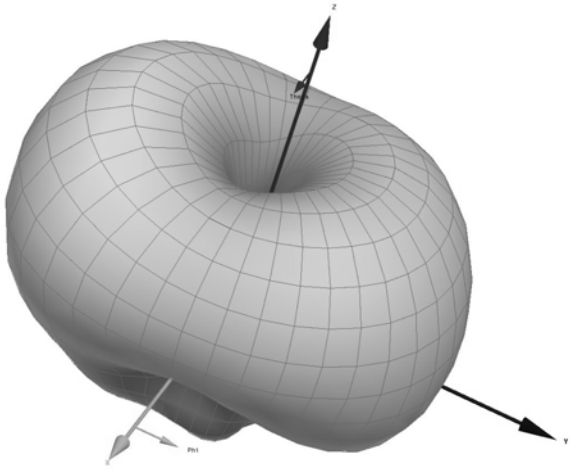
CPW line length $l$: 1 mm

The simulation results for a soda lime glass substrate are plotted in Figure 5.53. The monopole shows resonance at a frequency of 85GHz, and the far-field radiation pattern shows an omnidirectional and quite symmetric pattern, as expected.

The characteristic impedance calculation of CPW line, return loss and radiation pattern simulation of the monopole have been performed by Pan [108].




(a)



(b)

***Figure 5.53.*** *Simulation results: (a) Input return loss; (b) Radiation pattern for the monopole on a soda lime glass [108].*

### 5.4.3 Fabrication and Measurement

A polymer core conductor fabrication technique has been adopted for the high-aspect-ratio monopole structure. A photodefinable epoxy, SU-8 (Microchem, Inc.), which is favorable for high-aspect-ratio micro patterning, is used for the monopole backbone, and electroplated gold is used for the electrical conductive path. The skin depth of gold in the W-band (75 GHz ~ 110 GHz) is in the range of 0.30 μm to 0.24 μm. In general, 5 times the skin depth is considered to be sufficient to minimize the RF conductor loss and thereby not degrade the electrical performance. In this case a gold layer of approximately 1.5 μm was used.

Figure 5.54 details the fabrication process. A chromium coated soda-lime glass (Telic Co.) is used as a substrate. Chromium is patterned for the monopole column definition using standard photolithography *(a)*. SU-8 epoxy (800 μm thick) is coated on the substrate to a thickness that will ultimately define the monopole height. The SU-8 is exposed to a UV source from the substrate side to obtain a uniform column latent pattern. Alternatively, a front side exposure can be used if the substrate is opaque (Si, GaAs, etc.) *(b)*. The latent pattern is developed. Metal deposition of titanium and copper using a DC sputterer is carried out to form a conformal seed layer. Thin SU-8 (5 μm) is spin-coated and patterned for the definition of the signal path as well as ground pads using proximity photolithography due to the uneven surface topography *(c)*. Gold of 2 μm thickness is uniformly electrodeposited through the bottom mold as well as over the column surface. The thin SU-8, the seed layer, and the bottom chromium layer are removed sequentially to complete the process *(d)*. For fabrication simplicity, a two-mask process has been

described above. In order to obtain more accurate bottom electrode dimensions for the signal and the ground lines, bottom line metallization can be performed separately from the monopole metallization with an additional mask step. Since the maximum temperature of any fabrication step is below 100 °C, the process is CMOS compatible and easily integrable with a variety of substrates. Figure 5.55a and 5.55b show a photomicrograph of a fabricated CPW-fed monopole antenna array (3×3) and an SEM

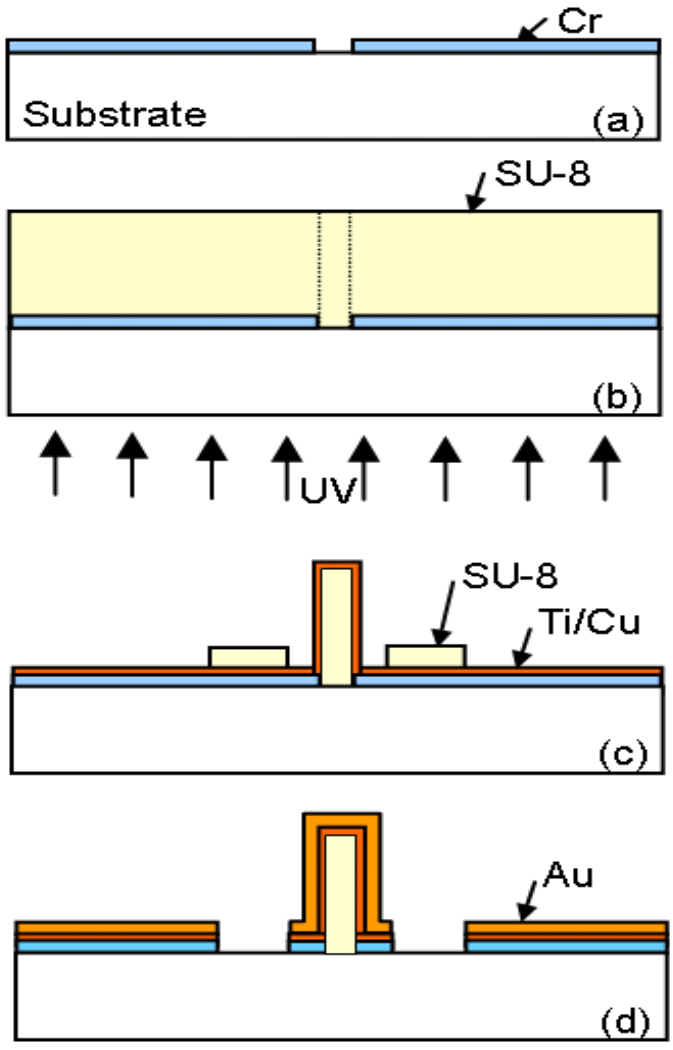
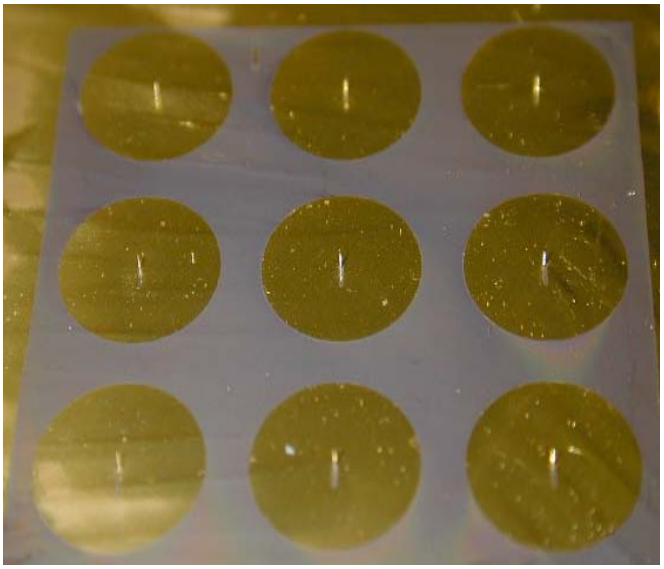


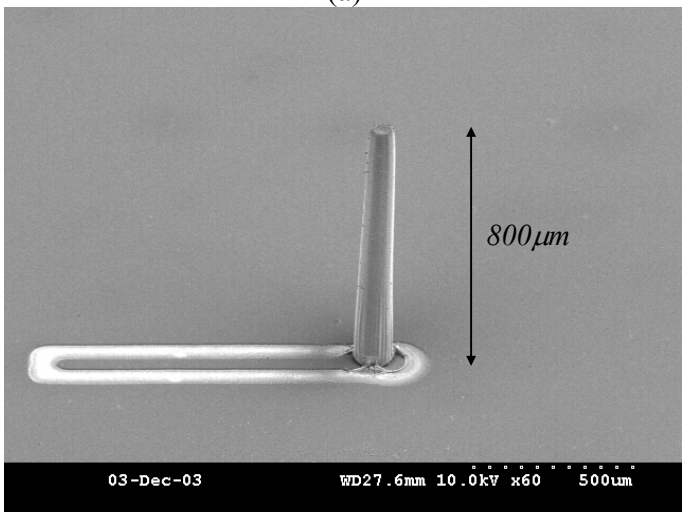

***Figure 5.54.*** *Fabrication process for monopole.*

image of a single monopole antenna, respectively. The fabricated structure is measured to be approximately 800 μm tall.

An Agilent 8510C vector network analyzer connected to a Cascade GSG 150 probe station has been used for s-parameter measurement after a standard SOLT calibration between 50 GHz and 110 GHz. Figure 5.56 shows measured and simulated return loss of



(a)




(b)

***Figure 5.55.*** *Fabricated CPW fed monopole antenna: (a) Photomicrograph of 3X3 monopole array; (b) An SEM image of 800μm tall monopole.*

a single monopole antenna from 50 GHz to 110 GHz. The measurements have been performed with a monopole with a height of 800 μm. A return loss of 16 dB was measured for the monopole resonating at 85 GHz. Good agreement between simulation and measurement is observed for the 800 μm tall sample. Radiation pattern measurements are currently underway.

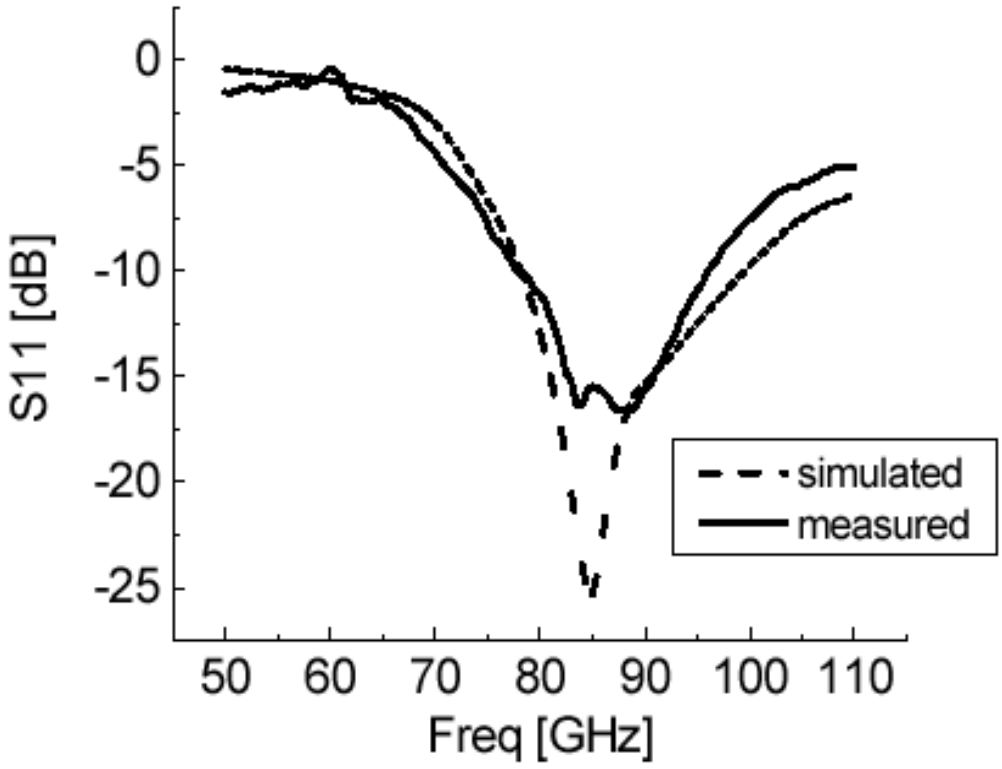



***Figure 5.56.*** *Measured and simulated reflection power (S11) for a monopole with a pole height of 800 μm.*

### 5.4.4 Summary and Discussion

A previously-developed epoxy core conductor fabrication concept is extended to millimeter wave applications with radiating structures. To demonstrate the process feasibility, a W-band micromachined monopole, which is vertically mounted on a glass substrate, is reported. A 2-D to 3-D feeding scheme is also proposed and optimized by simulation using a high frequency system simulator. Both the simulation and measurement results agree well. A return loss of 16 dB has been measured for a monopole of 800 μm thick, resonating at 85 GHz. This micromachined monopole, as well as more complex geometries based on the developed fabrication technologies, may have application in low-cost broadband compact millimeter wave communication systems.

# CHAPTER VI

# CONCLUSIONS

## 6.1. Summary

The research objective of this thesis was to develop electrical components for RF systems using 3-D MEMS fabrication technologies and advanced architectures. Integrated micro inductors, variable capacitors, and millimeter wave radiating structures were fabricated to demonstrate the feasibility and usefulness of the MEMS processes developed towards this end.

In the first portion of the thesis, various surface micromachining fabrication techniques for 3-D structures were discussed which were based on the manipulation of the photodefinable epoxy SU-8 and subsequent metallization. The fabrication processes were categorized into 5 sections: an embedded conductor, an epoxy-core conductor, a reverse-side exposure process, a multi-exposure process, and an inclined exposure patterning. Embedded conductor technology was based on using SU-8 as a via mold and leaving it as a part of the final structure, by which mechanically strong and package-

compatible metal conductors were fabricated with relative ease and short processing time, while simultaneously maintaining CMOS-compatibility constraints. Epoxy-core conductors were implemented by photopatterning epoxy as an underlying scaffold followed by metallization on the scaffold; using this approach, high-aspect-ratio RF conductors were fabricated very efficiently. Tall (~1 mm), high-aspect-ratio (~10:1) vertical interconnects were achieved. In the case of optically transparent substrates a reverse-side exposure technique gave an additional degree of freedom of patterning to the process, by which improved high-aspect-ratio (~20:1) photo patterning and self-alignment patterning were facilitated. Combining this approach with substrate optics showed the potential for useful structures such as tapered microneedles or pillars. Multi-exposure-single-develop techniques were used to fabricate bridges or channels. The thickness control for the top portion was done by control of baking steps. The usage of different UV sources was proposed for better thickness control. SU-8 patterning using inclined exposure was demonstrated for an integrated vertical screen filter. Laser ablation combined with inclined patterning produced more complicated 3-D structures such as microvasculature. Advanced 3-D structures combined with subsequent metallization (i.e. epoxy-core conductor) will help implement complicated RF components.

In the second part of this thesis, two architectures were introduced for RF components: a reduced intermodulation distortion (IMD) capacitor and a compact tunable LC module. By adding separate high resistivity electrodes within a wide RF gap, low IMD and large tuning at low tuning voltage was achieved. Various reduced IMD architectures were compared and summarized. A compact tunable LC module was

implemented by forming a ferroelectric gap capacitor in a spiral inductor shape, by which the overall device footprint was reduced.

In the third part, five RF components were fabricated using the developed fabrication processes and architectures: an embedded inductor; a high-aspect-ratio inductor using an epoxy-core conductor; a BST tunable gap capacitor with low-loss conductor; a reduced IMD capacitor; and a millimeter wave monopole antenna. The embedded inductor was implemented based on an embedded conductor. RF inductors with Q-factor of 15~20 and inductance of 0.8~2.6 nH at the frequency range of 1 ~ 5 GHz on a silicon substrate were fabricated. Successful integration of embedded inductors on a CMOS power amplifier was demonstrated. High-aspect-ratio inductors using the epoxy-core conductor process were fabricated on a glass substrate. Air core inductors with a height of 500 μm ~ 900 μm showed Q-factor of 31 ~ 84 and inductance of 0.5 ~ 2.5 nH at a frequency range of 1 ~ 5 GHz. A BST ferroelectric tunable capacitor was fabricated on a transparent sapphire substrate using a reverse-side exposure, self-alignment technique, by which a capacitor with a narrow gap of 1.2 μm and a thick electrode of 2.2 μm was fabricated. The capacitor showed improved Q-factor of 21.5 at 1 GHz compared with that of a 0.2 μm thick capacitor, 9.3 with tunability as large as 33 % at 10 V. Reduced IMD capacitors were fabricated to prove its concept. Fabrication processes with various high resistivity oxide conductors such as ITO, LSCO, AZO were successfully developed. The capacitors with single pair and double pair high resistivity structure show third-order input intercept point (IIP3) improvement of 6 dB and 15 dB compared to a narrow gap capacitor with tunability of 21 % at 30V for all three capacitors. A quarter-wave monopole antenna for W-band usage was successfully

fabricated using an epoxy-core conductor process. The height and the diameter of the monopole were 800 μm and 80 μm, respectively, radiating at 85 GHz with a return loss of 16 dB.

## 6.2. Future Work

The developed fabrication processes in this thesis are believed to be useful for RF passive components as well as millimeter wave applications. One way to more fully demonstrate their usefulness is to build these devices in an integrated fashion. Since the demonstrated fabrication processes using 3-D polymer and metallization are all low temperature ones and compatible with standard Si or GaAs circuit processes, it is imperative to implement them with other circuitry. In this thesis, one example of integration with RF embedded inductors and a CMOS power amplifier has been demonstrated. However, additional integration examples such as high Q-factor RF inductor integrated on a VCO or a mixer are expected. The combination of different inductors and capacitors can produce many other useful devices such as a matching circuit, a filter, and a resonator. While a compact LC module has been introduced, further combination is expected. A large potential area of the developed fabrication processes is in the area of millimeter wave and terahertz frequencies, since the characteristic size in the frequency range and the implementable device size fall in the same region, i.e., several tens to thousands of microns. Numerous radiating structures, waveguides, or cavity resonating structures will be appropriate future applications.

## 6.3. Conclusions

This thesis includes various 3-D fabrication techniques, architectures, and their applications for RF component implementation. High-aspect-ratio and complex 3-D fabrication techniques were developed using polymer patterning and its metallization. The concept of epoxy-core conductors is especially suitable for RF component fabrication, by which not only RF passive components but also millimeter wave components can be efficiently and economically fabricated. Combining it with complex 3-D fabrication techniques make it feasible to fabricate unique and unconventional micro structures for millimeter wave or terahertz frequency applications. The reduced IMD architecture for the ferroelectric tunable capacitor provides a solution for high power linear RF applications. The combination of the developed fabrication technologies, with each other as well as with integrated circuit and electronic packaging technologies, are expected to find great utility in future RF systems.

# BIBLIOGRAPHY

[1] Clark T.-C. Nguyen, Linda P.B. Katehi, and Gabriel M. Rebeiz, "Micromachined Devices for Wireless Communications," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1756 – 1768, 1998.

[2] Robert C. Frye, Peter R. Smith, and Yee L. Low, "Inductive Crosstalk Between Integrated Passive Components in RF-Wireless Modules," *1998 International Conference on Multichip Modules and High Density Packaging*, pp. 496 – 500, 1998.

[3] 'http://public.itrs.net/"

[4] Felix K. Schwering, "Millimeter Wave Antennss," *Proceddings of the IEEE,* vol. 80, no. 1, pp. 92-102, January, 1992.

[5] Gabriel M. Rebeiz, "Millimeter-Wave and Terahertz Integrated Circuit Antennas," *Proceddings of the IEEE,* vol. 80, no. 11, pp. 1748-1770, November, 1992.

[6] Warren L. Stutzman and Gary A. Thiele, *Antenna Theory and Design*, John Wiley & Sons, Inc., New York, 1998.

[7] David M. Pozar, "Considerations for Millimeter Wave Printed Antennas," *IEEE Trans. Antennas and Propagation*, vol. AP-31, no. 5, pp. 740-747, September, 1983.

[8] J.P. Papapolymerou, R.F. Drayton, and L.P.B. Katehi, "Micromachined Patch Antennas," *IEEE Trans. Antennas and Propagation*, vol. 46, no. 2, pp. 275-283, February, 1998.

[9] Gildas P. Gauthier, Jean-Pierre Raskin, Linda P.B. Katehi, Gabriel M. Rebeiz, “A 94-GHz Aperture-Coupled Micromachined Microstrip Antenna,” *IEEE Trans. Antennas and Propagation*, vol. 47, no. 12, pp. 1761-1766, December, 1999.

[10] G.M. Rebeiz, D.P. Kasilingam, P.A. Stimson, Y. Guo, and D.B. Rutledge, “Monolithic millimeter-wave two-dimensional horn imaging arrays,” *IEEE Trans. Antennas and Propagation*, vol. 28, pp. 1473-1482, September, 1990.

[11] R. M. Warner Ed., *Integrated Circuits: Design Principles and Fabrication*. New York: McGraw-Hill, 1965.

[12] E. Pettenpaul, "CAD models of lumped elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 294-304, 1988.

[13] Y. Imai, M. Tokumitsu, and A. Minakawa, "Design and performance of low current GaAs MMICs for L-band front-end applications," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 209-215, 1991.

[14] N. M. Nguyen and R. G. Meyer, "Si IC-Compatible Inductors and LC Passive Filters," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 1028-1031, 1990.

[15] J. Craninckx and M. S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 736-744, 1997.

[16] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 743-752, 1998.

[17] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2-um CMOS RF Amplifier," *IEEE Electron Device Letters,* vol. 14, pp. 246-248, 1993.

[18] J. M. Lopez-Willegas, J. Samitier, C. Cane, P. Losantos, and J. Bausells, "Improvement of the Quality factor of RF Integrated Inductors by Layout Optimization," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, pp. 76-83, 2000.

[19] M. Ozgur, M. E. Zaghloul, and M. Gaitan, "Optimization of Backside Micromachined CMOS Inductors for RF Applications," *IEEE International Symposium on Circuits and Systems,* pp. 185-188, 2000.

[20] S. Jenei, S. Decoutere, K. Maex, and B. Bauwelaers, "Add-on Cu/SiLKT$^{M}$ Module for High Q Inductors," *IEEE Electro Device Letters,* vol. 23, pp. 173-175, 2002.

[21] J. Park and M. Allen, "High Q Spiral-Type Microinductors on Silicon Substrates," *IEEE Trans. Magnetics,* vol. 135, pp. 3544-3546, 1999.

[22] Y.-J. Kim and M. G. Allen, "Surface Micromachined Solenoid Inductors for High Frequency Applications," *IEEE Trans. Components, Packaging, and Manufacturing Technology,* vol. Part C, 21, pp. 26-33, 1998.

[23] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, "Surface Micromachined Solenoid On-Si and On-Glass Inductors for RF Applications," *IEEE Electron Device Letters,* vol. 20, pp. 487-489, 1999.

[24] Y.-H. Joung, S. Nuttinck, S.-W. Yoon, M.G. Allen, and J. Laskar, "Integrated inductors in the chip-to-board interconnect layer fabricated using solderless electroplating bonding," *IEEE International Microwave Symposium Digest*, vol. 3, pp. 1409-1412, 2002.

[25] J. Zou, J. Chen, and C. Liu, "Plastic Deformation Magnetic Assembly (PDMA) of 3D Microstructures: Technology Development and Application," *Proceeding of the 11$^{th}$ International Conference on Solid-State Sensors and Actuators*, vol. 2, pp. 1582-1585, 2001.

[26] G.W. Dahlmann, E.M. Yeatman, P. Young, I.D. Robertson, and S. Lucyszyn, "High Q Achieved in Microwave Inductors Fabricated by Parallel Self-Assembly," *Proceeding of the 11th International Conference on Solid-State Sensors and Actuators*, vol. 2, pp. 1098-1101, 2001.

[27] C. L. Chua, D. K. Fork, K. V. Schuylenbergh, and J.-P. Lu, "Self-Assembled Out-Of-Plane High Q Inductors," *Proceedings of Solid-State Sensor, Actuator, and Microsystems workshop,* Hilton Head Is. SC, June 2-6, 2002, pp. 372-373.

[28] P. Penfield and R. P. Rafuse, V*aractor Applications.* Cambridge Mass: MIT Press, 1962.

[29] M. J. Howes and D. V. Morgan, "Variable Impedance Devices," John Wiley & Sons, 1978.

[30] G. W. Eldridge, M. C. Driver, M. M. Sopira, and T. J. Smith, "A High-Capacitiance Ratio Implanted MMIC Varactor for Broadband Phase Shifters and Tuners," *Technical Digest of 12th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium,* pp. 97-100, 1990.

[31] F. Hui, Z. Chen, K. Shen, J. Lau, M. Huang, M. Chan, P. K. Ko, G. Jin, and P. C. H. Chan, "High-Q SOI Gated Varactor for Use in RF ICs," *Proceedings of IEEE International SOI Conference,* pp. 31-32, 1998.

[32] D. Galt, T. Rivkina, and M. W. Cromar, "Microwave Tuning Quality and Power Handling of Voltage-Tunable Capacitors: Semiconductor Varactors versus Ba1-xSrxTiO3 Films," *Mat. Res. Soc. Symp. Proc.,* vol. 493, pp. 341-346, 1997.

[33] K.S. Tang, W.S. Lau, and G.S. Samudra, “Trends in DRAM Dielectrics,” *Circuits and Devices*, pp. 27-34, 1997.

[34] A. Tombak, J.-P. Maria, F. Ayguavives, Z. Jin, G. T. Stauf, A. I. Kingon, and A. Mortazawi, "Tunable Barium Strontium Titanate Thin Film Capacitors for RF and Microwave Applications," *IEEE Microwave and Wireless Components Letters,* vol. 12, pp. 3-5, 2002.

[35] R. York, A. Nagra, E. Erker, T. Taylor, P. Periaswamy, J. Speck, S. Streiffer, and O. Auciello, "Microwave Integrated Circuits using Thin-Film BST," *International Symposium on Applications of Ferroelectrics,* pp. 195-200, 2000.

[36] Dongsu Kim, Yoonsu Choi, M.G. Allen, J.S. Kenney, D. Kiesling, "A wide-band reflection-type phase shifter at S-band using BST coated substrate," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2903-2909.

[37] J. Zou, C. Liu, J. Schutt-Aine, J. Chen, and S.-M. Kang, "Development of a Wide Tuning Range MEMS Tunable Capacitor for Wireless Communication Systems," I*nternational Electron Device Meeting,* pp. 403-406, 2000.

[38] A. Dec and K. Suyama, "RF Micromachined Varactors with Wide Tuning Range," *IEEE MTT-S Digest,* pp. 357-360, 1998.

[39] G. V. Ionis, A. Dec, and K. Suyama, "Differential Multi-Finger MEMS Tunable Capacitors for RF Integrated Circuits," *IEEE MTT-S Digest,* vol. 1, pp. 345-348, 2002.

[40] R.L. Borwick III, P.A. Stupar, J.F. DeNatale, R. Anderson, R. Erlandson, "Variable MEMS capacitors implemented into RF filter systems," *IEEE Trans. Microwave Theory and Techniques*, vol. 51, no. 1, pp. 315-319, January 2003.

[41] F. W. V. Keuls, C. H. Mueller, F. A. Miranda, R. R. Romanofsky, C. L. Canedy, S. Aggarwal, T. Venkatesan, R. Ramesh, J. S. Horwitz, W. Chang, and W. J. Kim, "Room Temperature Thin Film $Ba_xSr_{1-x}TiO_3$ Ku-Band Coupled Microstrip Phase Shifters:

Effects of Film Thickness, Doping, Annealing and Substrate Choice," *IEEE MTT-S Digest,* pp. 737-740, 1999.

[42] M. S. Tsai, S. C. Sun, and T. Y. Tseng, "Effect of Oxygen to Argon Ratio on Properties of (Ba,Sr)TiO3 Thin Films Prepared by Radio-Frequency Magnetron Sputtering," *J. Appl. Phys.,* vol. 82, pp. 3482-3487, 1997.

[43] T. S. Kim, C. H. Kim, and M. H. Oh, "Structural and Electrical properties of RF Magnetron-Sputtered $Ba1_{-xS}rx_{T}iO3$ Thin Films on Indium-Tin-Oxide-Coated Glass Substrate," *J. Appl. Phys.,* vol. 75, pp. 7998-8003, 1994.

[44] S. S. Shoup, S. Shanmugham, D. Cousins, A. T. Hunt, M. Paranthaman, A. Goyal, P. Martin, and D. M. Kroeger, "Low-cost Combustion Chemical Vapor Deposition of Epitaxial Buffer Layers and Superconductors," *IEEE Trans. Applied Superconductivity,* pp. 2426-2429, 1999.

[45] D. Tahan, A. Safari, and L. C. Klein, "Sol-gel Preparation of Barium Strontium Titanate Thin Films," *Proceedings of IEEE International Symposium on Applications of Ferroelectrics,* pp. 427-430, 1994.

[46] W. J. Kim, W. Chang, S. B. Qadri, J. M. Pond, S. W. Kirchoefer, J. S. Horwitz, and D. B. Chrisey, "Structural and Microwave Properties of (Ba,Sr)TiO3 Films Grown by Pulsed Laser Deposition," *Appl. Phys,* vol. A 70, pp. 313-316, 2000.

[47] B. Acikel, Y. Liu, A. S. Nagra, T. R. Taylor, P. J. Hansen, J. S. Speck, and R. A. York, "Phase Shifters using (Ba,Sr)TiO3 Thin Films on Sapphire and Glass Substrates," *IEEE MTT-S Digest,* pp. 1191-1194, 2001.

[48] J.C. Maxwell, “A dynamical theory of the electromagnetic field,” *Proc. Royal Soc. (London)*, vol. 13, p.531, 1864.

[49] H. Hertz, "Ueber sehr schnelle electrische Schwingungen," *Wied. Ann.*, vol. 31, p. 421, 1887.

[50] Ronold W.P. King, "The Linear Antenna-Eighty Years of Progress," *Proc. The IEEE*, vol. 55, no. 1, pp. 2-16, 1967.

[51] Ronold W.P. King, Shantnu R. Mishra, Kuan M. Lee, Glenn S. Smith, "The Insulated Monopole: Admittance and Junction Effects," *IEEE Trans. Antennas and Propagation*, vol. AP-23, no. 2, pp. 172-177, 1975.

[52] James S. Mclean, "A Re-examination of the Fundamental Limits on the Radiation Q of Electrically Small Antennas," *IEEE Trans. Antennas and Propagation*, vol. 44, no. 5, pp. 672-676, May 1996.

[53] H.D. Foltz, J.S. Mclean, and G. Crook, "Disk-loaded Monopoles with Parallel Strip Elements," *IEEE Trans. Antennas and Propagation*, vol. 46, no. 12, pp. 1894-1896, December 1998.

[54] David M. Pozar, "Considerations for Millimeter Wave Printed ntennas," *IEEE Trans. Antennas and Propagation*, vol. AP-31, no. 5, pp. 740-747, 1983.

[55] J. R. James, P.S. Hall, and C. Wood, *Microstrip Antennas: Theory and Design*, Stevenage, U.K.: Peter Peregrinus, 1981, pp. 51-64.

[56] N.G. Alexopoulos and I.E. Rana, "Mutual impedance computation between printed dipoles," *IEEE Trans. Antennas and Propagation*, vol. AP-29, no. 1, pp. 106-111, January 1981.

[57] M.J. Vaughan, K. Hur, and R.C. Compton, "Improvement of microstrip patch antenna radiation patterns," *IEEE Trans. Antennas and Propagation*, vol. 42, pp. 882-885, June 1994.

[58] Gildas P. Gauthier, Jean-Pierre Raskin, Linda P.B. Katehi, Gabriel M. Rebeiz, "A 94-GHz Aperture-Coupled Micromachined Microstrip Antenna," *IEEE Trans. Antennas and Propagation*, vol. 47, no.12, pp. 1761-1766, December 1999.

[59] Ioannis Papapolymerou, Rhonda Franklin Drayton, and Linda P.B. Katehi, "Micromachined Patch Antennas," *IEEE Trans. Antennas and Propagation*, vol. 46, no. 2, pp. 275-283, February 1998.

[60] H. Ekstrom, S. Gearhart, P.R. Acharva, G.M. Rebeiz, E.L. Looberg, S. Jacobsson, "348-GHz endfire slotline antennas on thin dielectric membranes," *IEEE Microwave Guided Wave Lett*., vol. 2, pp. 357-358, September 1992.

[61] Steven S. Gearhart and Theodore Willke, "Integrated Antennas and Filters Fabricated using Micromachining Techniques," *Proceedings on Aerospace Conference*, pp. 249-254, 1998.

[62] John W. Digby, Caroline E. McIntosh, Geoff M. Parkhurst, Brian M. Towlson, Silas Hadjiloucas, John W. Bowen, J. Martyn Chamberlain, Roger D. Pollard, Robert E. Miles, D. Paul Steenson, Lucas S. Karatzas, Nigel J. Cronin, and Steve R. Davies, "Fabrication and Characterization of Micromachined Rectangular Waveguide components for Use at Millimeter-Wave and Terahertz Frequencies," *IEEE Trans. Microwave Theory and Techniques*, vol. 48, no. 8, pp. 1293-1302, August 2000.

[63] Editorial, "Back to the Future: Copper Comes of Age," *IBM Research*, vol. 35, 1997.

[64] A. Bruno Frazier and Mark G. Allen, "High Aspect Ratio Electroplated Microstructures Using a Photosensitive Polyimide," *Proceeding of IEEE Micro Electromechanical Systems*, 1992, pp. 87-92.

[65] T.M. Linkopoulos, Zhang Wenjin, and C.H. Ahn, "Electroplated thick CoNiMnP permanent magnet arrays for micromachined magnetic device applications," *Proceeding of IEEE Micro Electromechnical Systems*, 1996, pp. 79-84.

[66] C. Keller and M. Ferrari, "Milli-Scale Polysilicon Structures," *in Technical Digest of 1994 Solid State Sensor and Actuator Workshop*, Hilton Head Island, S.C., 1994, pp. 132-137.

[67] C.G. Keller and R.T. Howe, "Nickel-Filled Hexsil Thermally Actuated Tweezers," *in 8th International Conference on Solid-State Sensors and Actuators* (Transducers '95), June 1995, Stockholm, Sweden, pp. 376-379.

[68] Florent Cros, Kieun Kim, and Mark G. Allen, "A Single-Mask Process for Micromachined Magnetic Devices," *in Technical Digest of 2000 Solid State Sensor and Actuator Workshop*, Hilton Head Island, S.C., 2000, pp. 138-141.

[69] Yeun-Ho Joung, Electroplating Bonding Technology for Chip Interconnect, Wafer Level Packaging and Interconnect Layer Structures, Ph.D. Thesis, Georgia Institute of Technology, Fall 2003.

[70] M. Despont, H. Lorenz, N. Fahrni, J. Brugger, P. Renaud, and P. Vettiger, "High-Aspect-Ratio, Untrathick, Negative-Tone Near-UV Photoresist for MEMS Applications," *Proceedings of the IEEE Microelectromechanical Systems*, pp. 518-522, 1997.

[71] H. Lorenz, M. Despont, N. Fahrni, J. Brugger, P. Vettiger, P. Renaud, "High-aspect-ratio, ultrathick, negative-tone near-UC photoresist and its applications for MEMS," *Sensors and Actuators*, A 64, pp. 33-39, 1998.

[72] H. Lorenz, M. Despont, N. Fahrni, N. LaBianca, P. Renaud, and P Vettiger, "SU-8: a low-cost negative resist for MEMS," *J. Micromech. Microeng*. vol. 7, pp. 121-124, 1997.

[73] Yong-Kyu Yoon, Mark G. Allen, and Andrew T. Hunt, "Tunable Ferroelectric Capacitor with Low-Loss Electrodes Fabricated Using Reverse Side Exposure," *Proceedings of 53rd IEEE Electronic Components and Technology Conference (ECTC),* New Orleans, USA, pp.1534-1540, 2003.

[74] Jung-Hwan Park, Yong-Kyu Yoon, Mark R. Prausnitz, and Mark G. Allen, "High-Aspect-Ratio Tapered Structure using an Integrated Lens Technique," *Proceedings of IEEE Micro Electro Mechanical Systems (MEMS)*, Maastricht, the Netherlands, pp.383-386, 2004.

[75] Yoonsu Choi, R. Powers, V. Vernekar, A. B. Frazier, M. LaPlaca, and M.G. Allen, "High Aspect Ratio SU-8 Structures for 3-D Culturing of Neurons," *Proceedings of ASME International Mechanical Engineering Congress and Exposition*, Nov. 2003**.**

[76] W.E. Feely, J.C. Imhof, and C.M. Stein, "The Role of the Latent Image in a New Dual Image, Aqueous Developable, Thermally Stable Photoresist," *Polym. Eng. Sci.*, vol. 26, pp. 1101-1104, 1986.

[77] W.E. Feely, "Micro-Structures," *Technical Digest of Solid State Sensor and Actuator Workshop*, Hilton Head Island, S.C. pp. 13-15, 1988.

[78] P. Six, "Phase Masks and Grey-tone Masks," *Semiconductor Fabtech*, 1995.

[79] Jun-Bo Yoon, Bon-Kee Kim, Chul-Hi Han, Euisik Yoon, Kwyro Lee, and Choogn-Ki Kim, "High-Performance Electroplated Solenoid-Type Integrated Inductor ($SI^2$) for RF Applications Using Simple 3D Surface Micromachining Technology," *Technical Digest of International Electron Devices Meeting (IEDM '98)*, pp. 544-547, 1998.

[80] Jae-Duk Lee, Jun-Bo Yoon, Jae-Kwan Kim, Hoon-Ju Chung, Choon-Sup Lee, Hi-Deok Lee, Ho-Jun Lee, Choong-Ki Kim, and Chul-Hi Han, "A Thermal Inkjet Printhead

with a Monolithically Fabricated Nozzle Plate and Self-Aligned Ink Feed Hole," *J. Microelectromechnical Systems (MEMS)*, vol. 8, no. 3, pp. 229-236, 1999.

[81] F.G. Tseng, Y.J. Chuang, and W.K. Lin, "A Novel Fabrication Method of Embedded Micro Channels Employing simple UV Dosage Control and Antireflection Coating," *Proceedings of IEEE Microelectromechanical Systems (MEMS)*, pp. 69-72, 2002.

[82] http://www.microchem.com

[83] P. Bley, J. Gottert, M. Harmening, M. Himmelhaus, W. Menz, J. Mohr, C. Muller, and U. Wallrabe, "The LIGA Process for the Fabricaton of Micromechanical and Mirooptical Components," in Krahn, Reichl, ed., *Micro System Technologies 91* (Berlin 1991), pp. 302-314, 1991.

[84] W. Ehrfeld and A. Schmidt, "Recent Developments in Deep X-Ray Lithography," *J. Vac. Sci. Technol.*, vol. B16, pp. 3526-3534, 1998.

[85] O. Tabata, K. Terasoma, N. Agawa, and K. Yamamoto, "Moving Mask LIGA ($M^2$LIGA) Process for Control of Side Wall Inclination," *Proceedings of IEEE Microelectromechanical Systems (MEMS)*, pp. 252-256, 1999.

[86] C. Beuret, G.-A. Racine, J. Gobet, R. Luthier, and N.F. de Rooij, "Microfabrication of 3D Multidirectional Inclined Structures by UV Lithography and Electroplating," *Proceedings of IEEE Microelectromechanical Systems (MEMS)*, pp. 81-85, 1994.

[87] M. Han, W. Lee, S.-K. Lee, S.S. Lee, "Fabrication of 3D Microstructures with Inclined/Rotated UV Lithography," *Proceedings of IEEE Microelectromechanical Systems (MEMS)*, pp. 554-557, 2003.

[88] Yong-Kyu Yoon, Jung-Hwan Park, Florent Cros, and Mark G. Allen, "Integrated Vertical Screen Microfilter System Using Inclined SU-8 Structures," *Proceeding of IEEE Micro Electro Mechanical Systems (MEMS)*, Kyoto, Japan, pp.227-230, 2003.

[89] H. Sato, T. Kakinuma, J.S. Go, and S. Shoji, "A Novel Fabrication of In-channel 3-D Micromesh Structure Using Maskless Multi-Angle Exposure and Its Microfilter Application," *Proceeding of IEEE Micro Electro Mechanical Systems (MEMS)*, Kyoto, Japan, pp.223-226, 2003.

[90] S. Arscott, F. Garet, P. Mounaix, L. Duvillaret, J.-L Coutaz, and D. Lippens, "Terahertz Time-Domain Spectroscopy of Films Fabricated from SU-8," *Electronics Letters*, vol. 35, no. 3, pp. 243-244, 1999.

[91] Yong-Kyu Yoon, Richard Powers, Yoonsu Choi, Christophe Courcimault, and Mark G. Allen, "Micromachined Polymeric Microvasculatures: A Three-Dimensional Microfluidic System Using Inclined SU-8 Structures and Laser Machining," *Presented in 226$^{th}$ American Chemical Society National Meeting in Polymer division,* New York, NY, September 7-11, 2003.

[92] C.H. Mueller, R.R. Romanofsky, and F.A. Miranda, "Ferroelectric thin film & broadband satellite systems," *IEEE Potentials,* vol.20, no.2, pp.36-39, April-May 2001.

[93] Yong-Kyu Yoon, Dongsu Kim, Mark G. Allen, and J. Stevenson Kenney, "A Reduced Intermodulation Distortion Tunable Ferroelectric Capacitor: Architecture and Demonstration," *International Microwave Symposium Digest of IEEE MTT-S*, vol. 3, June 8-13, 2003, pp. 1989-1992.

[94] Yong-Kyu Yoon, Dongsu Kim, Mark G. Allen, J. Stevenson Kenney, and Andrew T. Hunt, "A Reduced Intermodulation Distortion Tunable Ferroelectric Capacitor-

Architecture and Demonstration," *IEEE Trans. Microwave Theory and Techniques, vol. 51, no. 12, December 2003,* pp.2568-2576.

[95] Ashok Chalaka, "Packaging Technology: Integrated Passive Devices," *Magazine of Passive Component Industry*, Mar/April 2000.

[96] B. Lakshminaravanan, T. Weller, "Tunable bandpass filter using distributed MEMS transmission lines," *IEEE MTT-S International Microwave Symposium, Digest*, vol. 3, June 8-13, 2003, pp. 1789-1792.

[97] N.J. Pulsford, J.T.M. Van Beek, M.H.W.M. Van Delden, A. Boogaard, R.F. Milsom, "Passive integration on Si for RF circuits in wireless applications," *IEEE MTT-S International Microwave Symposium*, Digest, vol. 4, June 13-19, 1999, pp. 1897-1900.

[98] MEMCAD, Coventor, Inc. (http://www.coventor.com)

[99] Y. Emery Chen, Yong Kyu Yoon, Joy Laskar, and Mark Allen, "A 2.4GHz Integrated CMOS Power Amplifier with Micromachined Inductors", *International microwave symposium digest, 2001 IEEE MTT-S, v*ol. 1, pp. 523-526, 2001.

[100] L.E. Cross and R.E. Newnham, Ceramics and Civilization, vol. III, High Technology Ceramics-Past, Present, and Future, *The American Ceramic Society, Inc.*, pp. 289-305, 1987.

[101] S.S. Gevorgian and E.L. Kollberg, "Do we really need ferroelectrics in paraelectric state only in electrically controlled microwave devices?" *Asian-pacific Microwave Conference*, December 3-6, 2000, pp. 917-922.

[102] C.H.Mueller, F.W. Van Keuls, R.R.Romanofsky, F.A.Miranda, "Ferroelectric and SiGe device development for high data rate communications," *Asia-Pacific Microwave Conference*, December 3-6, 2000, pp.923-928.

[103] G. Subramanyam, A. Zaman, N. Mohsina, F.W. Van Keuls, F.A. Miranda, R. R. Romanofsky, "A Narrow-Band Ferroelectric Tunable Bandpass Filter for K-Band Applications," *Asia-Pacific Microwave Conference*, December 3-6, 2000, pp.938-941.

[104] N.J. Wu, H. Lin, K. Xie, X.Y. Li, L. Jia, and A. Ignatiev, "Study of $Ba_{1-x}Sr_xTiO_3$ (100) epitaxial thin films prepared by laser deposition," *Proceedings of the 9th IEEE International Symposium on Applications of Ferroelectrics,* 1994, pp. 464-467.

[105] Yong-Kyu Yoon, Jin-Woo Park, and Mark G. Allen, "RF MEMS Based on Epoxy-Core Conductors," *Digest of Solid-State Sensor, Actuator, and Microsystems Workshop 2002*, Hilton Head Island, South Carolina, pp.374-375, 2002

[106] Warren L. Stutzman and Gary A. Thiele, *Antenna Theory and Design*, Chapter 2 and 5, John Wiley & Sons, Inc., New York, 1998.

[107] R.F. Schwartz, "Input Impedance of a Dipole of Monopole," *Microwave Journal*, vol. 15, p.22, Dec. 1972.

[108] Bo Pan, Yong-Kyu Yoon, Peter Kirby, John Papapolymerou, Manos M. Tentzeris, and Mark G. Allen, "A W-band surface micromachined monopole for low-cost wireless communication systems," will be published in the Proceedings of International Microwave Symposium, Fort Worth, TX, June 6-11, 2004.

# VITA

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